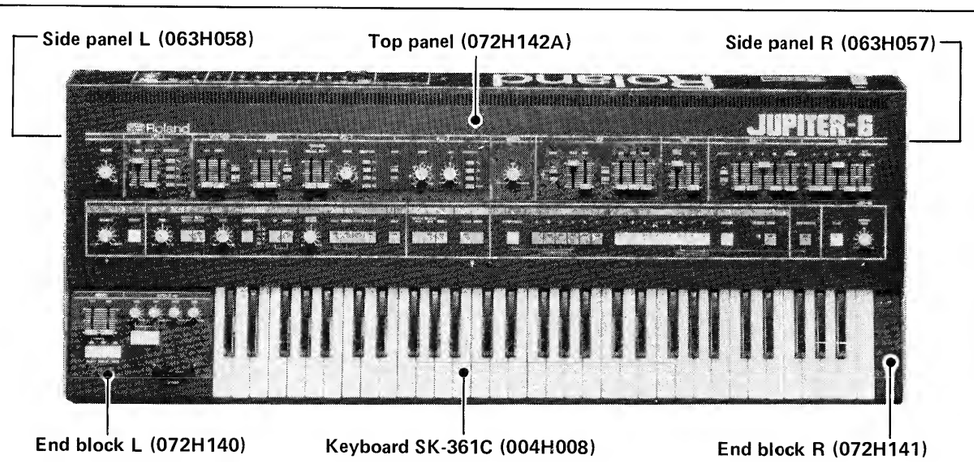
JP-6

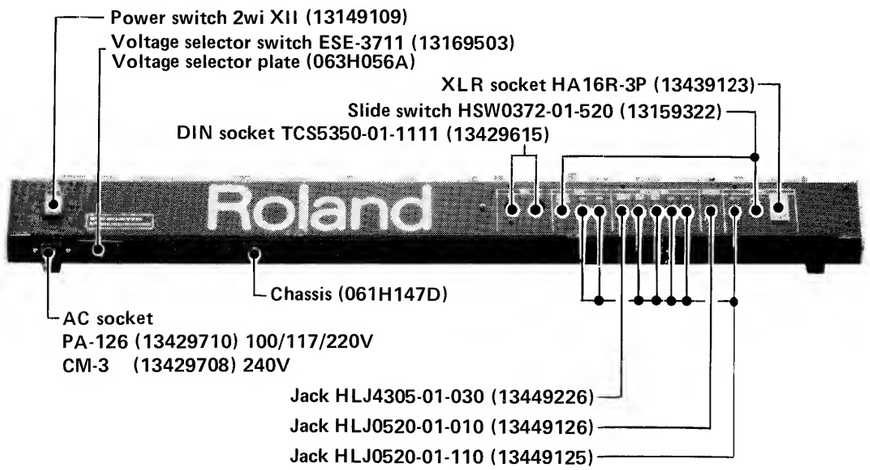
SERVICE NOTES

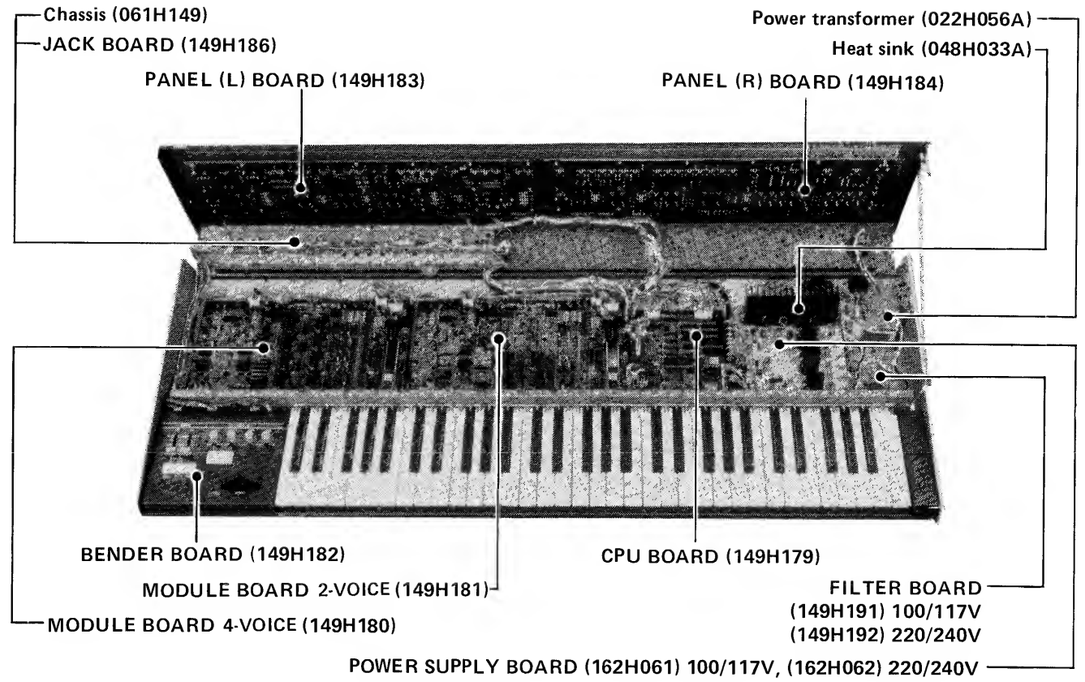
First Edition

SPECIFICATIONS

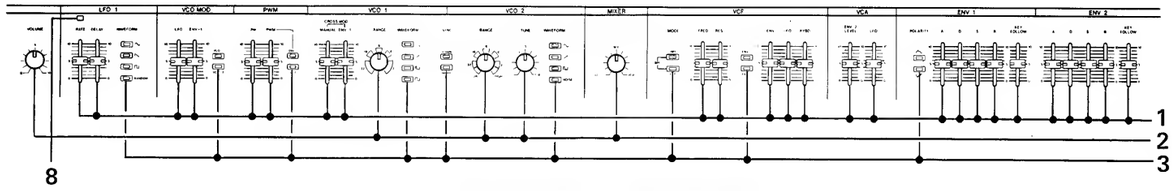
KEYBOARD	61 keys, 5 octaves, C scale
MASTER TUNE	±50 cents
VCO MOD	LFO 10 oct; ENV-1 5 oct
PWM	50-0%
VCF	LPF 24dB; HPF 24dB; BPF 12dB Cutoff frequency 5Hz-30kHz ENV more than 10 octaves LFO more than 10 octaves Key Follow 0-120%
VCA	ENV-2 Level 60dB max.
ENV-1	Attack Time 18s max.
(VCO, VCF, PWM)	Decay Time 20s max. Release Time 20s max. Key Follow 0-120%
ENV-2	Attack Time 18s max.
(VCF, VCA)	Decay Time 20s max. Release Time 20s max. Key Follow 0-120%
LFO-1	Rate 0.04-100Hz; Random 0.04-400Hz Delay Time 0-2s
LFO-2	VCO Sens more than ±100 cents VCF Sens ±4 oct; Rise Time 50ms-1s
ARPEGGIO	Rate 1-25Hz; Range 1, 2, 3, 4 octaves
GLIDE	Time 0-1.6s/oct
BENDER	Range greater than 3 oct Up/Down VCO Sens ±1 oct; VCF sens ±5 oct
OUTPUT	1/4 phone jack 0/–15/–30dB XLR impedance 600 ohms Headphones 8 ohms, stereo
EXTERNAL CONT	Arpeggio 1 step/clock (more than 2.5V) VCA –20dB; VCF –6 to +2 oct
POWER CONSUMPTION	30 watts
DIMENSIONS	1063(W) x 434(D) x 120(H)mm 41-7/8(W) x 17-1/16(D) x 4-3/4(H)in
WEIGHT	16 kg 35 lb 4 oz



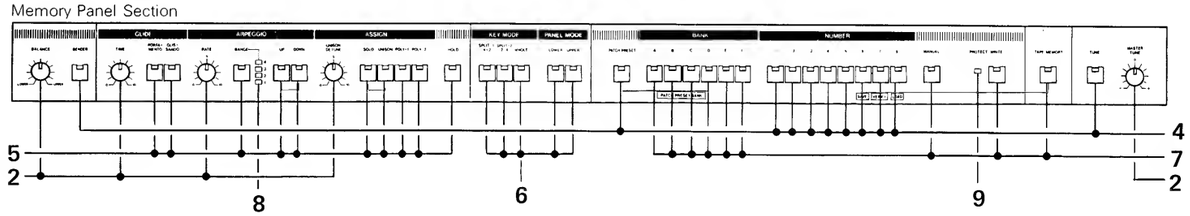


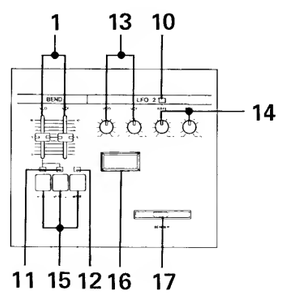


Manual Control Section



Memory Panel Section



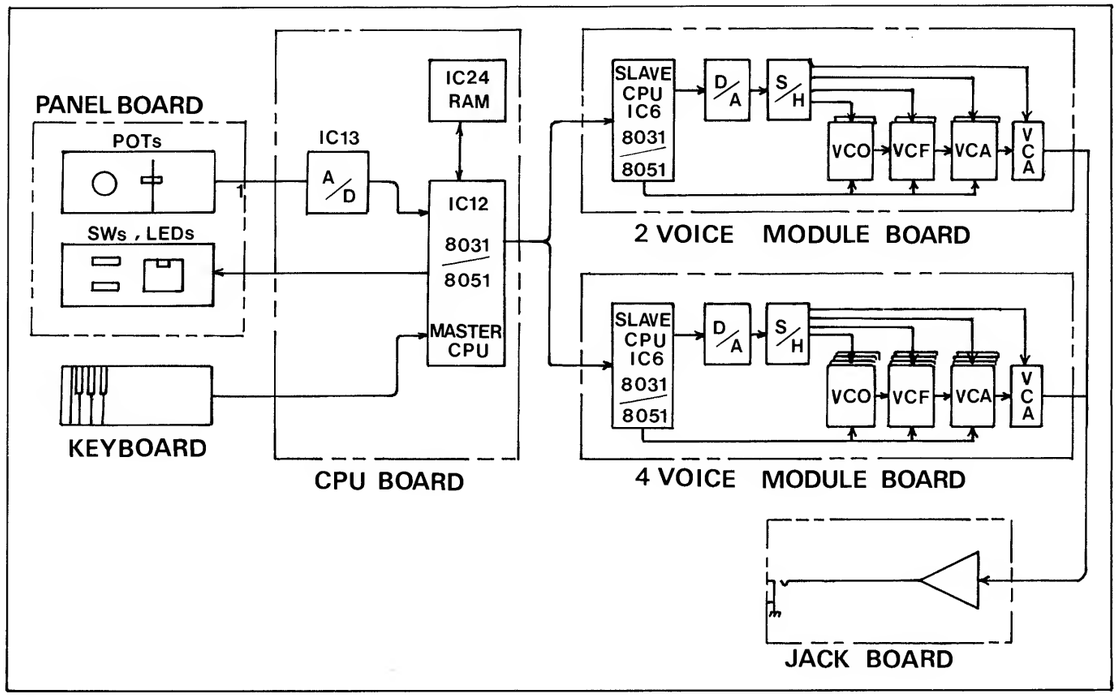


1. Pot S3018P405-B15 100kB (13339421), Knob (016H098)
2. Pot EVH-5XAP15-B15 100kB (13219126), Knob (016H102)
3. Button (016H095)
4. Button (016H085)
5. Button (016H086)
6. Button (016H087)
7. Button (016H088)

   Switch SPQ009F (13129327)
   LED (See parts list)
8. LED GL-9HD12 (15029152)
9. LED GL-9ND2 (15029148)
10. LED GL-9PR12 (15029150)
11. LED GL-9PG12 (15029149)
12. LED GL-9HY12 (15029151)
13. Pot EVH-5XAP15-B14 10kB (13219125), Knob (016H106)
14. Pot EVH-5XAP15-B15 100kB (13219126), Knob (016H106)
15. Switch SUT32A-1 (13129531), Button (016H036)
16. Key switch ass'y KEH1003 (13129717)
17. Bender unit PB-6 (2327571300)

CIRCUIT DESCRIPTION

General



The setting values of the potentiometers on the PANEL BOARDs are converted into digital equivalent by the A/D converter (IC13) on the CPU BOARD, and are read by the MASTER CPU (IC12). The setting values of the switchies on the PANEL BOARDs are directly read by the CPU through the Matrix circuits divided into the two PANEL BOARDs. The CPU (IC12) writes these data into RAM (IC24). The data in the RAM are read by control operation through the panel when required and are fed to the CPUs (SLAVE CPUs) on the MODULE BOARDs in serial format.

The SLAVE CPUs control VCOs, VCFs and VCAs using the data (tone data, keyboard information, etc.) coming from the MASTER CPU.

The BENDER and foot pedal controls are processed by analog circuits. The SLAVE CPUs gate the right analog switches to pass these control voltages to individual destinations to introduce additional features.

MASTER CPU

IC12 (CPU BOARD) P8031/P8051/P8051-318

Difference Between CPUs

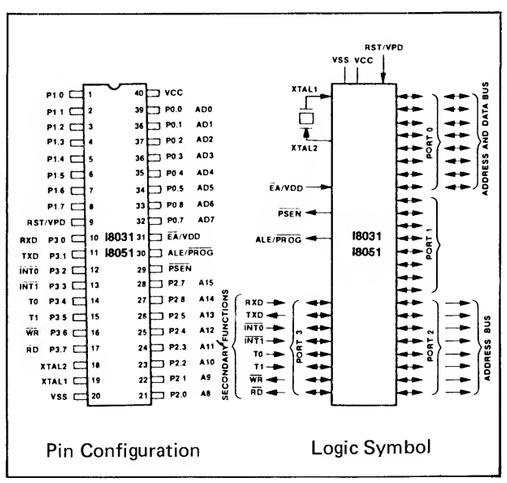
P8031 . . . . . .for early products, associated with PROM IC26 containing the operational program exclusive to the JP-6.

P8051 . . . . . .tentatively used. To be handled as P8031.

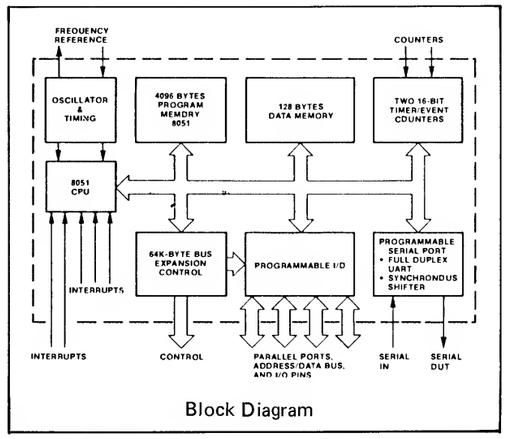
P8051-318 . . . . . .contains the program in the on-chip ROM, making IC26 redundant.

Compatibility

Three CPUs function the same as long as external PROM IC26 is enabled. Pulling up EA (pin 31) of P8051–318 will change programs from external to internal (see CPU circuit diagram), but this is unnecessary when IC26 operates perfectly.



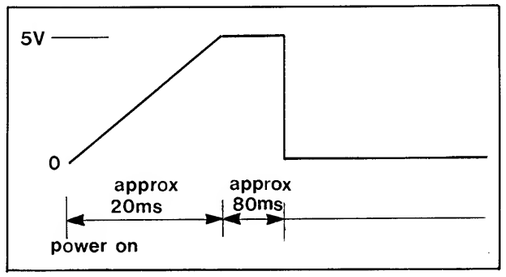
Pin Configuration Logic Symbol



Block Diagram

Pin Function

RST ..... The level of the reset terminal is kept high by RESET circuit (TR6, TR7, TR8 and IC21) for more than 24 clocks after the DC voltages becomes stable.



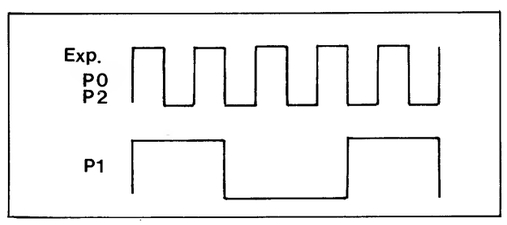
P0 ..... carries data and address data.

ALE ..... sends latch clock to IC17 to latch address off the P0 bus.

PSEN ..... enables IC26 to read a program in the PROM through the P0 bus.

P1 ..... serves as an I/O port.
It presents panel LED lighting, potentiometer and switch reading addresses.

P2 ..... issues addresses



RD ..... enables Read Address Decoder IC19 when the CPU wants to read necessary data. IC19 decodes select signals (P2.4-P2.6) and directs either of IC13, IC14, IC23, IC24, IC25 or IC27 to place data on the data bus.

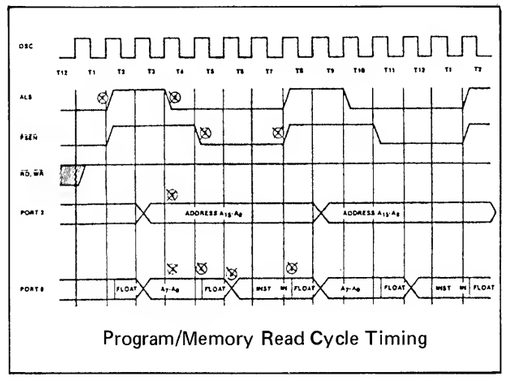
WR ..... enables Write Address Decoder IC18 which, upon decoding address being fed, clocks RAMs, A/D converter (IC13) and LED driver (IC15, IC16).

T0, T1, TX ..... transmit data to the cassette tape interface, MIDI bus and SLAVE CPUs.

RX ..... reads data from MIDI bus.

INT 1 ..... reads data from the cassette interface.

INT 0 ..... not used.



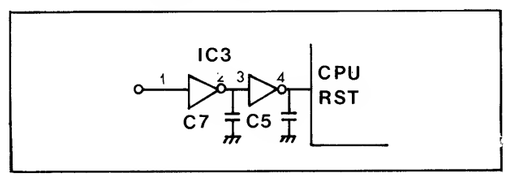
Program/Memory Read Cycle Timing

SLAVE CPU

IC6 (MODULE BOARD)

Compatibility ·· In the same way as IC12 on the CPU BOARD, P8031, P8051 or P8051-319 is used for the CPU (IC6). Refer to "MASTER CPU." P8051-319 makes IC1 and IC5 redundant.

RST ..... receives a shaped reset pulse from the CPU BOARD through buffers. The buffers (IC3) and capacitors (C5 and C7) effectively protect the CPU against static charge.



P0, P2, PSEN and ALE ···· Refer to the description in the MASTER CPU section.

P1 ..... delivers addresses to the S/H analog switches.

RD and INT 1 ·· clock the address latches (IC7, IC8) to ON or OFF analog switches.

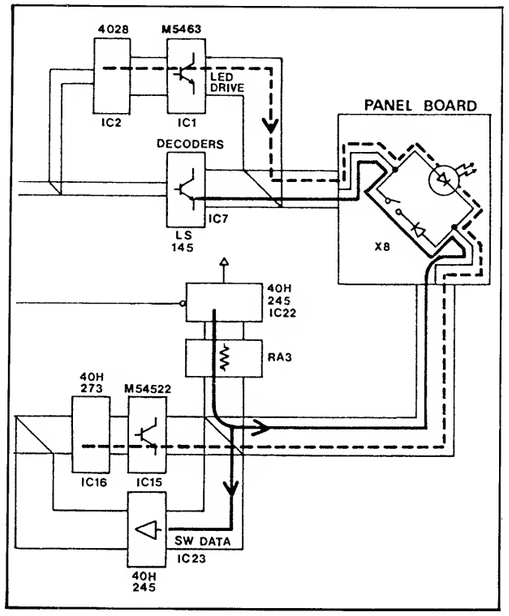
INT 0 ..... reads the frequencies of the VCOs during computune operation.

RX ..... accepts data from the MASTER CPU.

TX ..... goes high during Computune, signaling MASTER CPU not to send data.

T0, T1 ..... transmit LFO-LED lighting signals, and transmit and receive LFO sync pulses to and from the other SLAVE CPU.

Reading switch states and driving LEDs



Reading switch states and driving LEDs are alternately repeated through 8 x 8 matrix (divided into the R and L PANEL BOARDs) using a single line.

1. **Reading panel switch states**

Turned on by the CPU, IC22 pulls the bus positive through RA3. Simultaneously, a designated bit of IC7 is pulled low. A closed switch contact in the low bit effectively lowers one of input pins of IC23. The combination of bits (at IC7 output and IC23 input pins) informs the CPU which switch has been pressed not pressed.

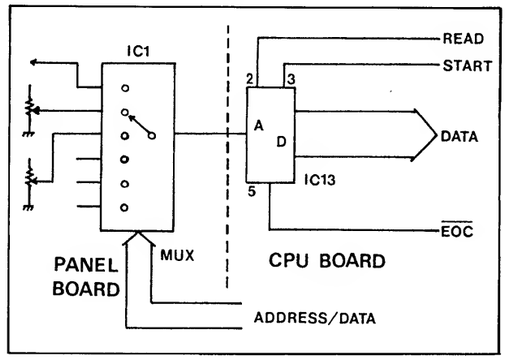
2. **Lighting LEDs**

IC22 is turned off by the CPU and the bus is now in a float state. At this time, IC2 (4028) decodes the applied address and has a high at the corresponding output of LED driver IC1.
When an output of IC16 goes high, a transistor in IC15 saturates, allowing one of the 8 LEDs (max) to be lit for 2ms.
The above-mentioned operations, reading of panel switch states and lighting of LEDs, are repeated eight times (one cycle).

Reading potentiometer data

IC1 (Multiplexer) sequentially connects Panel potentiometers to IC13 (A/D converter). IC13 starts conversion when signaled by START derived from IC18 (Write Address Decoder) with $\overline{WR}$.

After A/D conversion, $\overline{EOC}$ of IC13 goes low to inform the CPU of completion of conversion. Upon receiving the $\overline{EOC}$, the CPU outputs READ to accept the digital equivalent of a control setting.



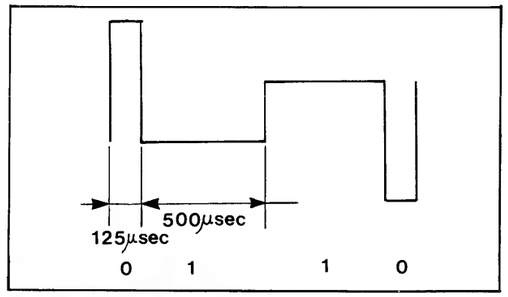
Cassette interface

SAVE

The CPU (IC12) converts data from the RAM (IC24) into two kinds of pulses with different widths (0 to 125μs and 1 to 500μs) as shown in the figure.
Accordingly, the average transmitting speed (signalling speed) is calculated as follows:

$$T = \frac{125 + 500\ (\mu s)}{2} = 312.5\mu s$$

$$\text{Thus} \quad \frac{1}{T(312.5)} = 3.2\text{k baud}$$



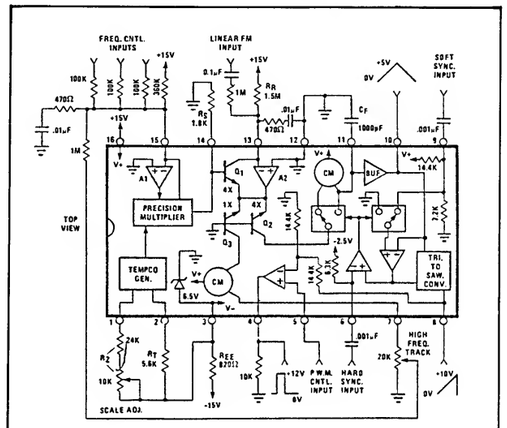
LOAD, VERIFY

IC4, TR2 and associated circuits shape the input signal from the cassette interface into a pulse wave. IC12 (CPU) reads the shaped waveform through INT 1 and measures the period between waveform edges to determine whether the data is 1 or 0.
When detecting an error by summation check, the program skips the block in which the error exists, lighting an indicator, then loads the next block. If there is no error through loading, the program returns to the normal mode. If an error occurs, error indicator(s) remain lit and the program cannot escape the TAPE mode until the TAPE button is pressed.

MODULE BOARD

VCO

Each VCO (IC33, IC36) is composed of a single chip IC, CEM3340. Three waveforms from the VCO are unequal in amplitude, which is compensated in the next stage (IC34 or IC37) for uniformed levels. Synchronization with the associated VCO is accomplished by external connections, leaving the internal SYNC disabled.



CEM 3340 Circuit Block and Connection Diagram

COMPUTUNE

When the TUNE button is pressed, the sawtooth wave selected among the outputs from the VCOs by IC20 passes through the comparator (IC4) then to CPU (IC6). The CPU measures the frequency of the wave and delivers a corrected CV data for that VCO to D/A converter IC11. The CPU repeats the cycle for the remainder of VCOs.

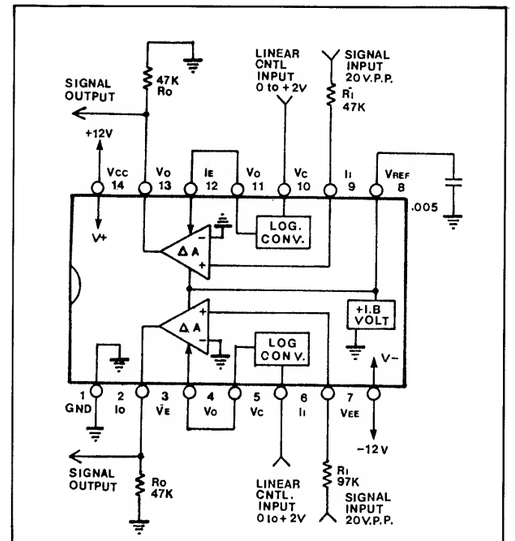
VCF

VCF is comprised of two seriese-connected filters of basically the some configuration. Each can function as either LPF or HPF of 12dB/oct slope when its output point is suitably selected.
Moreover the VCF will serve as a BPF by configuring one filter into LPF and the other HPF. In the JP-6 the 1st becomes HPF and 2nd LPF when VCF-MODE selectors are in BPF. Slight difference between two stages in circuit diagram illustrates compensation means for level and prevention against peak clips.

VCA

1st VCA

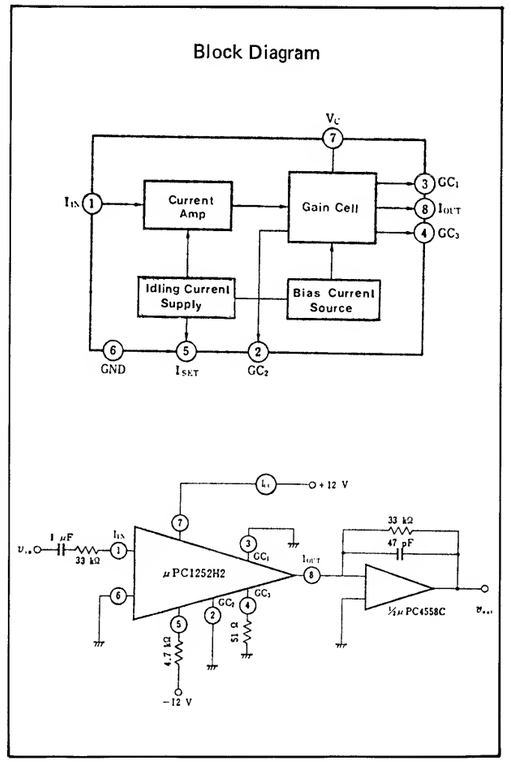
This device functions as a linear VCA accepting control signal through its linear control terminal.
The signal is called ENV–2, a combination of A, D, S, R and K.F data.



CEM 3360 Block Diagram and Typical Connection

2nd VCA

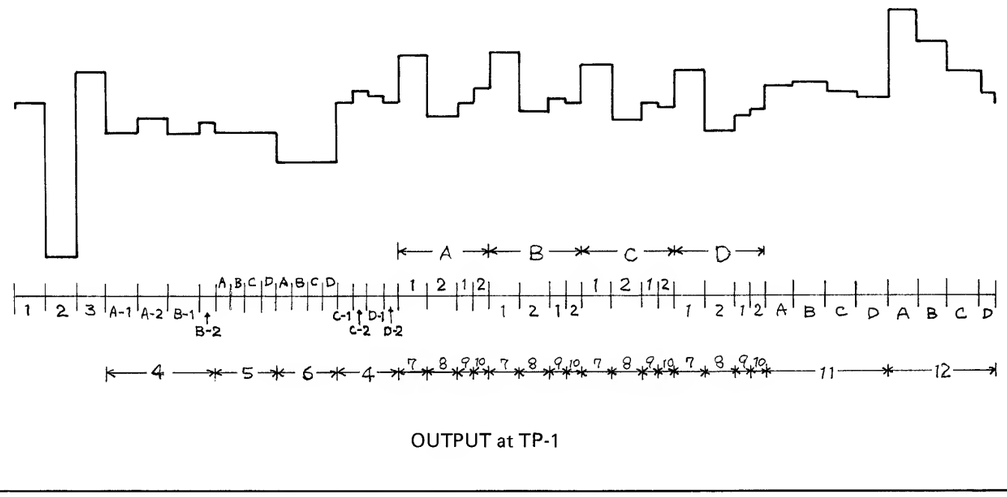
This device is controlled by the control knobs, VCA ENV-2 LEVEL and VCA LFO, and determines the entire output level of the MODULE BOARD.



MODULE CONTROL VOLTAGE

The SLAVE CPU IC6 routes the data to IC11 and has the serial analog equivalents (CVs) at IC12 output, TP-1. Connect the scope to the TP-1 (TRIG on TP-4 signal). The figures exampled below will appear on the screen, taking altogether approx. 2.6ms with amplitudes about 10.7V maximum. (The amplitude of each waveform will, of course, greatly differ from actual display being determined by a control setting.)

These D/A outputs are commonly distributed to S/Hs and are individually sampled into and held at desired output of the S/H.



OUTPUT at TP-1

Contents at S/H Outputs

Numbers are keyed to numbers in the figure above and headings to designation of S/H outputs.

1. MIX — Amount of MIX control.
2. RESO — Amount of RESO control.
3. M.VCA — Amount of VCA ENV-2 LEVEL and VCA LFO controls.

The above three controls are common to all the voices in a MODULE BOARD.

4. WIDTH — Computune (width) data for each VCO, ideally approximately 5V. It may vary with the characteristics of the VCO IC. If the value greatly differs from the ideal value, the corresponding VCO is judged to be defective, unless the computune operation is improper.
5. PWM — Amount of PWM controls (PW, PWM ENV-1 and PWM LFO) fro each VOICE (two VCOs).

Four (two) displayed waveforms will become distinguishable from each other when keys are played non-legato in POLY-1 with the following control settings:

PWM = 10; ENV-1: S = 10, R = 0, A and D = at small amount.

The settings are also applicable to 6.X–MOD and 11. VCF waveforms

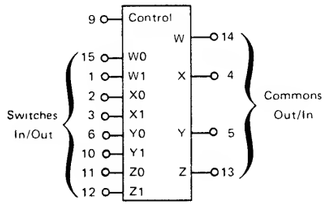
6. X-MOD — Amount of X-MOD controls (MANU, ENV–1).
7. CV 1 — Amount of CV (RANGE, LFO, KCV and TUNE) for VCO-1.
8. CV 2 — Amount of CV (the same parameters as for VCO-1) for VCO-2.
9. FREQ 1 — Computuned data (FREQ) and ENV MOD control for VCO-1.
10. FREQ 2 — Computuned data (FREQ) and ENV MOD control for VCO-2.
11. VCF — Amount of controls (FREQ, ENV, LFO and KYBD) to determine a cutoff point of VCF.
12. VCA — Amount of ENV-2 controls (A, D, S, R and K.F, except ENV-2 LEVEL) for the 1st VCA IC50.

IC DATA

MC14551B

QUAD 2-INPUT

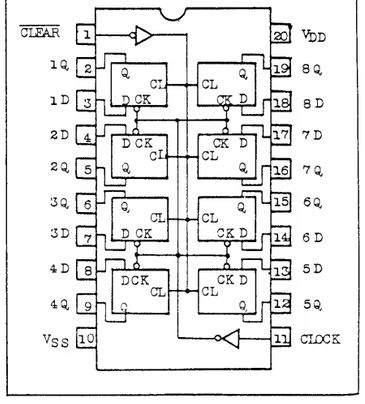
ANALOG MULTIPLEXER/DEMULTIPLEXER



Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Pin Configuration



TRUTH TABLE

INPUTS			OUTPUT
$\overline{CLEAR}$	CLOCK	DATA	Q
L	*	*	L
H	↑	H	H
H	↑	L	L
H	L	*	Qo

* = Don't care

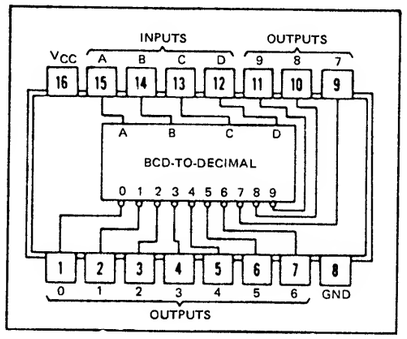
74LS145
BCD-TO-DECIMAL DECODERS/DRIVERS

FUNCTION TABLE

NO.	INPUTS D	C	B	A	OUTPUTS 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

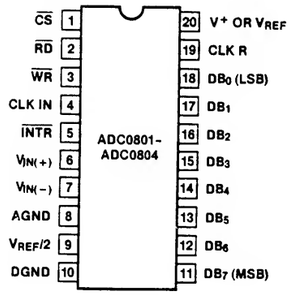
H = high level (off), L = low level (on)

(TOP VIEW)



ADC0803
A/D Converters

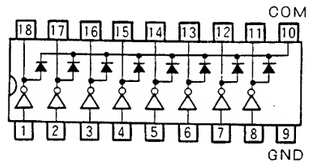
Pin Configuration



TOP VIEW

M54522P

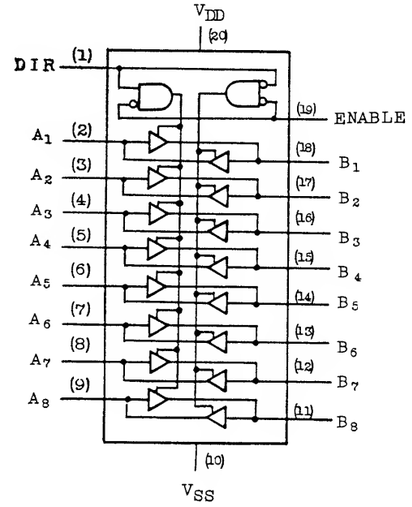
Pin Configuration



TOP VIEW

TC40H245P
OCTAL BUS TRANSCEIVERS
NONINVERTED 3-STATE OUTPUTS

Pin Configuration



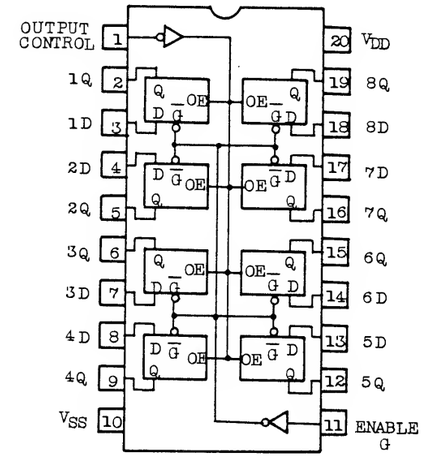
TRUTH TABLE

CONTROL INPUTS ENABLE	DIR	DATA PORT STATUS
L	L	B data to A bus
L	H	A data to B bus
H	X	High Impedance

X= Don't care

TC40H373P
OCTAL "D" TYPE LATCHES

Pin Configuration



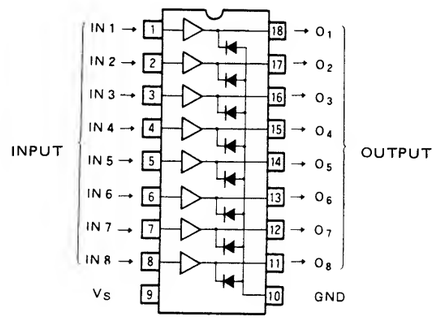
TRUTH TABLE

INPUTS OUTPUT CONTROL	ENABLE G	DATA	OUTPUT Q
L	H	H	H
L	H	L	L
L	L	*	Qo
H	*	*	High Impedance

*=Don't care

M54563P
8 UNIT 500mA SOURCE TYPE DARLINGTON TRANSISTOR ARRAY

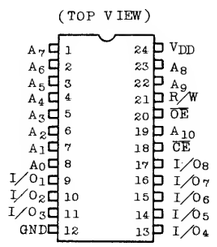
Pin Configuration



TOP VIEW

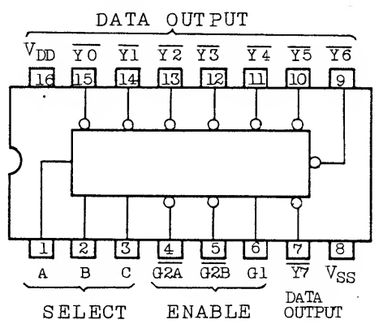
TC5517AP TC5517APL

Pin Configuration



TC40H138P
3-TO-8 LINE DECODER/MULTIPLEXER

Pin Configuration



TRUTH TABLE

INPUTS ENABLE G1	G2A	G2B	SELECT A	B	C	OUTPUTS Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	※	※	※	※	※	H	H	H	H	H	H	H	H
※	H	※	※	※	※	H	H	H	H	H	H	H	H
※	※	H	※	※	※	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

※ : Don't care

WIRING DATA TABLE

CPU BOARD

Pin No.	CON-NECTOR	CONTENTS	DESTINATION
1	CR3	PANEL IN 7	PANEL (R) BOARD RC3;10
2	CR3	PANEL IN 6	PANEL (R) BOARD RC3;9
3	CR3	PANEL IN 5	PANEL (R) BOARD RC3;8
4	CR3	PANEL IN 4	PANEL (R) BOARD RC3;7
5	CR3	PANEL IN 3	PANEL (R) BOARD RC3;6
6	CR3	PANEL IN 2	PANEL (R) BOARD RC3;5
7	CR3	PANEL IN 1	PANEL (R) BOARD RC3;4
8	CR3	PANEL IN 0	PANEL (R) BOARD RC3;3
9	CR3	PANEL BUTTON LED (R) 7	PANEL (R) BOARD RC3;2
10	CR3	D.GND	PANEL (R) BOARD RC3;1
11	CR1	PANEL BUTTON LED (R) 4	PANEL (R) BOARD RC1;18
12	CR1	PANEL BUTTON LED (R) 3	PANEL (R) BOARD RC1;17
13	CR1	PANEL BUTTON LED (R) 0	PANEL (R) BOARD RC1;16
14	CR1	PANEL POT (R) 4	PANEL (R) BOARD RC1;15
15	CR1	PANEL POT (R) 3	PANEL (R) BOARD RC1;14
16	CR1	PANEL POT (R) 2	PANEL (R) BOARD RC1;13
17	CR1	PANEL POT (R) 1	PANEL (R) BOARD RC1;12
18	CR1	PANEL POT (R) 0	PANEL (R) BOARD RC1;11
19	CR2	NC	
20	CR2	TO PANEL REF	PANEL (R) BOARD RC2;24
21	CR2	PANEL POT DATA IN	PANEL (R) BOARD RC2;23
22	CR2	PANEL PROTECT	PANEL (R) BOARD RC2;22
23	CR2	A.GND	PANEL (R) BOARD RC2;21
24	CR2	TO +15V	PANEL (R) BOARD RC2;20
25	CR2	TO −15V	PANEL (R) BOARD RC2;19
26	CJ	JACK HOLD	JACK BOARD JC;11
27	CJ	JACK PATCH	JACK BOARD JC;10
28	CJ	JACK ARP (SW)	JACK BOARD JC;9
29	CJ	JACK ARP CLOCK	JACK BOARD JC;8
30	CJ	CASSETTE OUT	JACK BOARD JC;7
31	CJ	CASSETTE IN	JACK BOARD JC;6
32	CJ	JACK PROTECT	JACK BOARD JC;5
33	CJ	MIDI IN	JACK BOARD JC;4
34	CJ	MIDI OUT	JACK BOARD JC;3
35	CJ	MIDI OUT	JACK BOARD JC;2
36	CJ	NC	
37	CM4	CLK OUT	MODULE BOARD MC;1
38	CM4	D.GND	MODULE BOARD MC;2
39	CM4	PANEL LFO LED	MODULE BOARD MC;3
40	CM4	PANEL LFO LED	MODULE BOARD MC;4
41	CM4	FROM MOD BUSSY	MODULE BOARD MC;5
42	CM4	RESET	MODULE BOARD MC;6
43	CM4	T1	MODULE BOARD MC;7
44	CM4	D.GND	MODULE BOARD MC;8
45	CP	+15V	POWER SUPPLY BOARD
46	CP	A.GND	POWER SUPPLY BOARD
47	CP	−15V	POWER SUPPLY BOARD
48	CP	REF (+10V)	POWER SUPPLY BOARD
49	CP	+5V (LED)	POWER SUPPLY BOARD
50	CP	D.GND	POWER SUPPLY BOARD
51	CP	+5V	POWER SUPPLY BOARD
52	CP	RESET	POWER SUPPLY BOARD
53	KC2	FROM KEYBOARD	
54	KC2	FROM KEYBOARD	
55	KC2	FROM KEYBOARD	
56	KC2	FROM KEYBOARD	
57	KC2	FROM KEYBOARD	
58	KC2	FROM KEYBOARD	
59	KC2	FROM KEYBOARD	
60	KC2	FROM KEYBOARD	
61	KC1	FROM KEYBOARD	
62	KC1	FROM KEYBOARD	
63	KC1	FROM KEYBOARD	
64	KC1	FROM KEYBOARD	
65	KC1	FROM KEYBOARD	
66	KC1	FROM KEYBOARD	
67	KC1	FROM KEYBOARD	
68	KC1	FROM KEYBOARD	
69	CL3	PANEL IN 7	PANEL (L) BOARD LC3;16
70	CL3	PANEL IN 6	PANEL (L) BOARD LC3;17
71	CL3	PANEL IN 5	PANEL (L) BOARD LC3;18
72	CL3	PANEL IN 4	PANEL (L) BOARD LC3;19
73	CL3	PANEL IN 3	PANEL (L) BOARD LC3;20
74	CL3	PANEL IN 2	PANEL (L) BOARD LC3;21
75	CL3	PANEL IN 1	PANEL (L) BOARD LC3;22
76	CL3	PANEL IN 0	PANEL (L) BOARD LC3;23
77	CL3	PANEL BUTTON LED 7	PANEL (L) BOARD LC3;24
78	CL3	D.GND	PANEL (L) BOARD LC3;25
79	CL1	PANEL BUTTON LED 6	PANEL (L) BOARD LC1;1
80	CL1	PANEL BUTTON LED 5	PANEL (L) BOARD LC1;2
81	CL1	PANEL BUTTON LED 0	PANEL (L) BOARD LC1;3
82	CL1	PANEL BUTTON LED 2	PANEL (L) BOARD LC1;4
83	CL1	PANEL BUTTON LED 1	PANEL (L) BOARD LC1;5
84	CL1	PANEL POT 3	PANEL (L) BOARD LC1;6
85	CL1	PANEL POT 2	PANEL (L) BOARD LC1;7
86	CL1	PANEL POT 1	PANEL (L) BOARD LC1;8
87	CL2	PANEL POT 0	PANEL (L) BOARD LC2;9
88	CL2	TO PANEL REF (+5V)	PANEL (L) BOARD LC2;10
89	CL2	PANEL POT DATA IN	PANEL (L) BOARD LC2;11
90	CL2	LFO LED	PANEL (L) BOARD LC2;12
91	CL2	A.GND	PANEL (L) BOARD LC2;13
92	CL2	TO +15V	PANEL (L) BOARD LC2;14
93	CL2	TO −15V	PANEL (L) BOARD LC2;15
94	CM2	CLOK OUT	MODULE BOARD 2 MC2;1
95	CM2	D.GND	MODULE BOARD 2 MC2;2
96	CM2	PANEL LFO LED	MODULE BOARD 2 MC2;3
97	CM2	PANEL LFO LED	MODULE BOARD 2 MC2;4
98	CM2	FROM MOD BUSSY	MODULE BOARD 2 MC2;5
99	CM2	RESET	MODULE BOARD 2 MC2;6
100	CM2	TO	MODULE BOARD 2 MC2;7
101	CM2	D.GND	MODULE BOARD 2 MC2;8

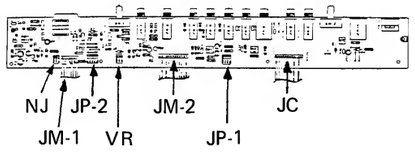
MODULE BOARD (4 VOICE)

Pin No.	CON-NECTOR	CONTENTS	DESTINATION
1	MC4	CLK IN	CPU BOARD CM4;37
2	MC4	D.GND	CPU BOARD CM4;38
3	MC4	LFO IN (T0)	CPU BOARD CM4;39
4	MC4	LFO IN (T1)	CPU BOARD CM4;40
5	MC4	TX	CPU BOARD CM4;41
6	MC4	RESET	CPU BOARD CM4;42
7	MC4	RX	CPU BOARD CM4;43
8	MC4	D.GND	CPU BOARD CM4;44
9	M4P-1	+5V	POWER SUPPLY BOARD
10	M4P-1	D.GND	POWER SUPPLY BOARD
11	M4P-1	A.GND	POWER SUPPLY BOARD
12	M4P-1	−15V	POWER SUPPLY BOARD
13	M4P-1	+15V	POWER SUPPLY BOARD
14	M4P-1	Ref (+10V)	POWER SUPPLY BOARD
15	M4P-2	−15V	POWER SUPPLY BOARD
16	M4P-2	−15V	POWER SUPPLY BOARD
17	M4P-2	A.GND	POWER SUPPLY BOARD
18	M4P-2	A.GND	POWER SUPPLY BOARD
19	M4P-2	+15V	POWER SUPPLY BOARD
20	M4P-2	+15V	POWER SUPPLY BOARD
21	M4J	NOISE IN	JACK BOARD JM1;40
22	M4J	A.GND	—
23	M4J	VCA OUT	JACK BOARD JM1;36
24	M4J	VCA CONT	JACK BOARD JM2;19
25	M4J	VCF CONT	JACK BOARD JM2;17
26	M4J	VCO BEND 2	JACK BOARD JM2;21
27	M4J	VCO BEND 1	JACK BOARD JM2;23

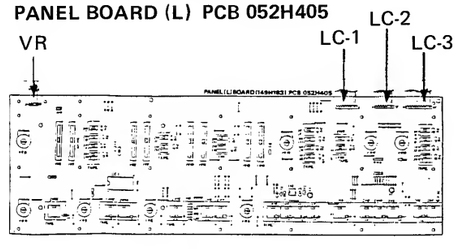
MODULE BOARD (2 VOICE)

Pin No.	CON-NECTOR	CONTENTS	DESTINATION
1	MC2	CLK IN	CPU BOARD CM2;94
2	MC2	D.GND	CPU BOARD CM2;95
3	MC2	LFO IN (T0)	CPU BOARD CM2;96
4	MC2	LFO IN (T1)	CPU BOARD CM2;97
5	MC2	TX	CPU BOARD CM2;98
6	MC2	RESET	CPU BOARD CM2;99
7	MC2	RX	CPU BOARD CM2.100
8	MC2	D.GND	CPU BOARD CM2;101
9	M2P-1	+5V	POWER SUPPLY BOARD
10	M2P-1	D.GND	POWER SUPPLY BOARD
11	M2P-1	A.GND	POWER SUPPLY BOARD
12	M2P-1	−15V	POWER SUPPLY BOARD
13	M2P-1	+15V	POWER SUPPLY BOARD
14	M2P-1	Ref (+10V)	POWER SUPPLY BOARD
15	M2P-2	−15V	POWER SUPPLY BOARD
16	M2P-2	−15V	POWER SUPPLY BOARD
17	M2P-2	A.GND	POWER SUPPLY BOARD
18	M2P-2	A.GND	POWER SUPPLY BOARD
19	M2P-2	+15V	POWER SUPPLY BOARD
20	M2P-2	+15V	POWER SUPPLY BOARD
21	M2J	NOISE IN	JACK BOARD JM1;41
22	M2J	A.GND	—
23	M2J	VCA OUT	JACK BOARD JM1;38
24	M2J	VCA CONT	JACK BOARD JM2;18
25	M2J	VCF CONT	JACK BOARD JM2;16
26	M2J	VCO BEND 2	JACK BOARD JM2;20
27	M2J	VCO BEND 1	JACK BOARD JM2;22

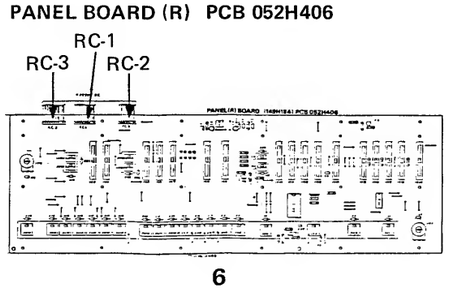
JACK BOARD PCB 052H408



PANEL BOARD (L) PCB 052H405



PANEL BOARD (R) PCB 052H406



PANEL (R) BOARD

Pin No.	CON-NECTOR	CONTENTS	DESTINATION	
1	RC3	D.GND	CPU BOARD	CR3;10
2	RC3	DECODER 7	CPU BOARD	CR3;9
3	RC3	BUS 0	CPU BOARD	CR3;8
4	RC3	BUS 1	CPU BOARD	CR3;7
5	RC3	BUS 2	CPU BOARD	CR3;6
6	RC3	BUS 3	CPU BOARD	CR3;5
7	RC3	BUS 4	CPU BOARD	CR3;4
8	RC3	BUS 5	CPU BOARD	CR3;3
9	RC3	BUS 6	CPU BOARD	CR3;2
10	RC3	BUS 7	CPU BOARD	CR3;1
11	RC1	PANEL POT 0	CPU BOARD	CR1;18
12	RC1	PANEL POT 1	CPU BOARD	CR1;17
13	RC1	PANEL POT 2	CPU BOARD	CR1;16
14	RC1	PANEL POT 3	CPU BOARD	CR1;15
15	RC1	PANEL POT 4	CPU BOARD	CR1;14
16	RC1	DECODER 0	CPU BOARD	CR1;13
17	RC1	DECODER 3	CPU BOARD	CR1;12
18	RC1	DECODER 4	CPU BOARD	CR1;11
19	RC2	−15V	CPU BOARD	CR2;25
20	RC2	+15V	CPU BOARD	CR2;24
21	RC2	A.GND	CPU BOARD	CR2;23
22	RC2	PANEL PROTECT	CPU BOARD	CR2;22
23	RC2	POT DATA	CPU BOARD	CR2;21
24	RC2	+5V (REF)	CPU BOARD	CR2;20

PANEL (L) BOARD

Pin No.	CON-NECTOR	CONTENTS	DESTINATION	
1	LC1	DECODER 6	CPU BOARD	CL1;79
2	LC1	DECODER 5	CPU BOARD	CL1;80
3	LC1	DECODER 0	CPU BOARD	CL1;81
4	LC1	DECODER 2	CPU BOARD	CL1;82
5	LC1	DECODER 1	CPU BOARD	CL1;83
6	LC1	PANEL POT OUT 3	CPU BOARD	CL1;84
7	LC1	PANEL POT OUT 2	CPU BOARD	CL1;85
8	LC1	PANEL POT OUT 1	CPU BOARD	CL1;86
9	LC2	PANEL POT OUT 0	CPU BOARD	CL2;87
10	LC2	REF (+5V)	CPU BOARD	CL2;88
11	LC2	VR DATA	CPU BOARD	CL2;89
12	LC2	LFO LED	CPU BOARD	CL2;90
13	LC2	A.GND	CPU BOARD	CL2;91
14	LC2	+15V	CPU BOARD	CL2;92
15	LC2	−15V	CPU BOARD	CL2;93
16	LC3	BUS 7	CPU BOARD	CL3;69
17	LC3	BUS 6	CPU BOARD	CL3;70
18	LC3	BUS 5	CPU BOARD	CL3;71
19	LC3	BUS 4	CPU BOARD	CL3;72
20	LC3	BUS 3	CPU BOARD	CL3;73
21	LC3	BUS 2	CPU BOARD	CL3;74
22	LC3	BUS 1	CPU BOARD	CL3;75
23	LC3	BUS 0	CPU BOARD	CL3;76
24	LC3	DECODER 7	CPU BOARD	CL3;77
25	LC3	D.GND	CPU BOARD	CL3;78
26	VR	POT IN	JACK BOARD	VR;28
27	VR	POT OUT	JACK BOARD	VR;30
28	VR	A.GND	JACK BOARD	VR;29

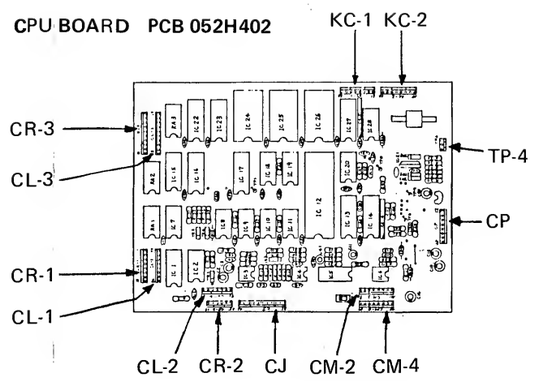
JACK BOARD

Pin No.	CONNECTOR	CONTENTS	DESTINATION	
1	JC	NC	–	
2	JC	MIDI OUT	CPU BOARD	CJ;35
3	JC	MIDI OUT	CPU BOARD	CJ;34
4	JC	MIDI IN	CPU BOARD	CJ;33
5	JC	MEMORY PROTECT	CPU BOARD	CJ;32
6	JC	CASSETTE IN	CPU BOARD	CJ;31
7	JC	CASSETTE OUT	CPU BOARD	CJ;30
8	JC	ARP.CLK	CPU BOARD	CJ;29
9	JC	ARP.CLK (SW)	CPU BOARD	CJ;28
10	JC	PATCH SHIFT	CPU BOARD	CJ;27
11	JC	PEDAL HOLD	CPU BOARD	CJ;26
12	JP1	+15V	POWER SUPPLY BOARD	
13	JP1	A.GND	POWER SUPPLY BOARD	
14	JP1	A.GND	POWER SUPPLY BOARD	
15	JP1	−15V	POWER SUPPLY BOARD	
16	JM2	VCF CONT (MODU 2)	MODULE BOARD 2	M2J;25
17	JM2	VCF CONT (MODU 4)	MODULE BOARD 4	M4J;25
18	JM2	VCA CONT (MODU 2)	MODULE BOARD 2	M2J;24
19	JM2	VCA CONT (MODU 4)	MODULE BOARD 4	M4J;24
20	JM2	BENDER VCO-2 (TO MODU 2)	MODULE BOARD 2	M2J;26
21	JM2	BENDER VCO-2 (TO MODU 4)	MODULE BOARD 4	M4J;26
22	JM2	BENDER VCO-1 (TO MODU 2)	MODULE BOARD 2	M2J;27
23	JM2	BENDER VCO-1 (TO MODU 4)	MODULE BOARD 4	M4J;27
24	JM2	FROM VCO-1 BENDER	BENDER BOARD	BJ;4
25	JM2	FROM VCO-2 BENDER	BENDER BOARD	BJ;5
26	JM2	FROM VCF BENDER	BENDER BOARD	BJ;6
27	JM2	NC		
28	VR	POT IN	PANEL BOARD (L)	VR;26
29	VR	A.GND	PANEL BOARD (L)	VR;28
30	VR	POT OUT	PANEL BOARD (L)	VR;27
31	JP2	RESET	POWER SUPPLY BOARD	
32	JP2	+15V	POWER SUPPLY BOARD	
33	JP2	A.GND	POWER SUPPLY BOARD	
34	JP2	A.GND	POWER SUPPLY BOARD	
35	JP2	−15V	POWER SUPPLY BOARD	
36	JM1	VCA OUT (MODU 4)	MODULE BOARD 4	M4J;23
37	JM1	A.GND	MODULE BOARD 4	M4J;22
38	JM1	VCA OUT (MODU 2)	MODULE BOARD 2	M2J;23
39	JM1	A.GND	MODULE BOARD 2	M4J;22
40	JM1	NOISE OUT (MODU 4)	MODULE BOARD 4	M4J;21
41	JM1	NOISE OUT (MODU 2)	MODULE BOARD 2	M2J;21
42	NJ	TO XLR (1)		
43	NJ	TO XLR (2)		
44	NJ	TO XLR (3)		

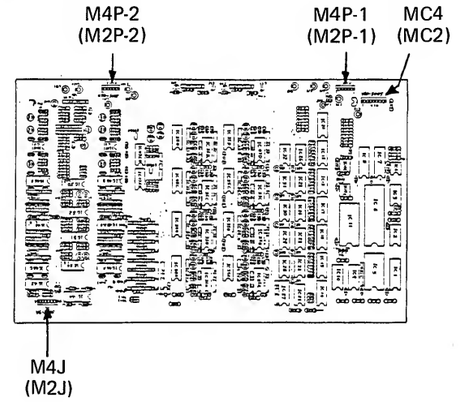
BENDER BOARD

Pin No.	CONNECTOR	CONTENTS	DESTINATION	
1	BP	A.GND	POWER SUPPLY BOARD	
2	BP	+15V	POWER SUPPLY BOARD	
3	BP	−15V	POWER SUPPLY BOARD	
4	BJ	VCO-1 CONT	JACK BOARD	JM2;24
5	BJ	VCO-2 CONT	JACK BOARD	JM2;25
6	BJ	VCF CONT	JACK BOARD	JM2;26
7	BJ	NC		
8	BE	A.GND	PB-6	
9	BE	−15V	PB-6	
10	BE	CONT	PB-6	
11	BE	+15V	PB-6	

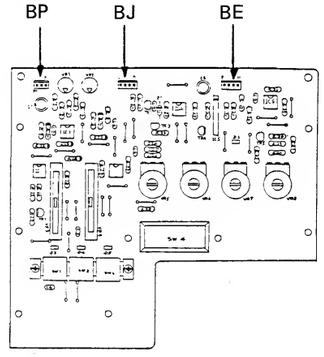
CPU BOARD PCB 052H402



MODULE BOARD 4 Voice (2 Voice) PCB 052H403



BENDER BOARD PCB 052H404



CPU BOARD

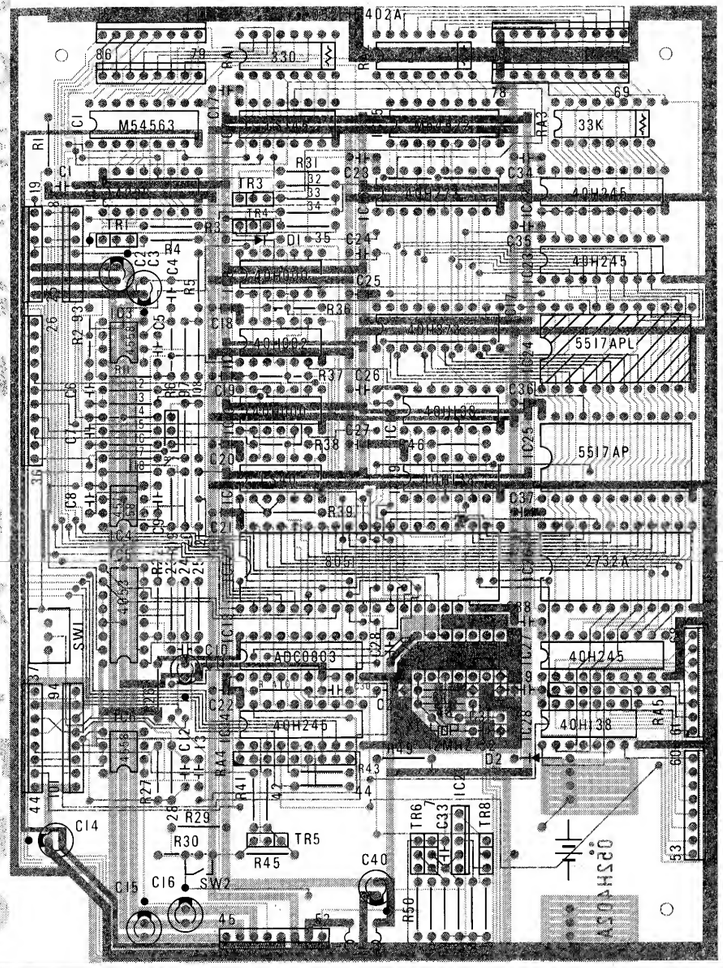
149H179 (PCB 052H402A)

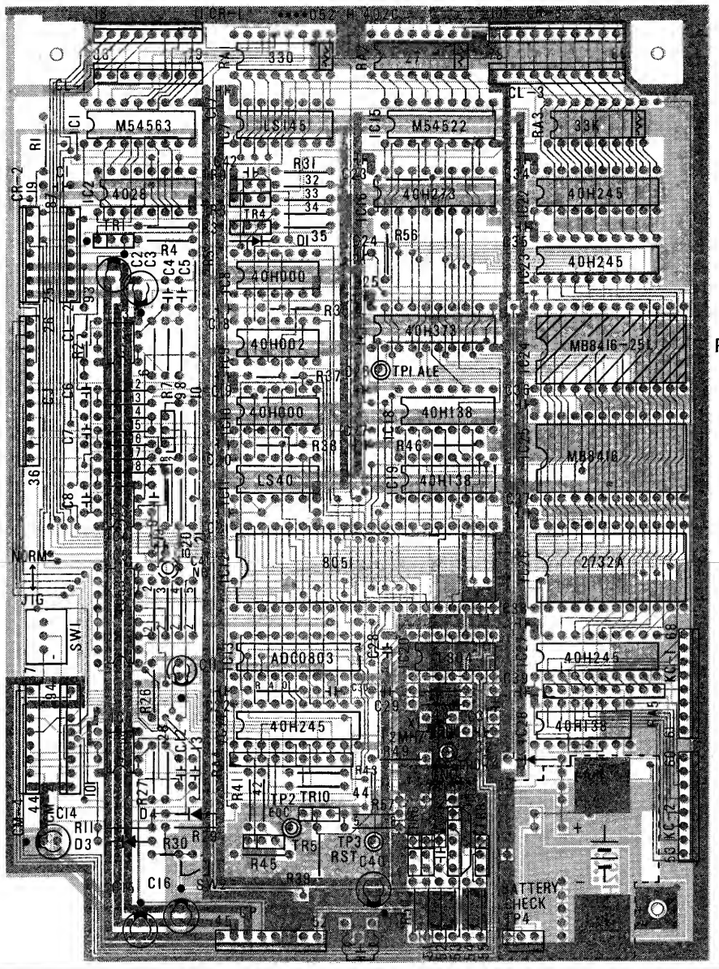
(PCB 052H402C) SERIAL NUMBER 311800 AND UP

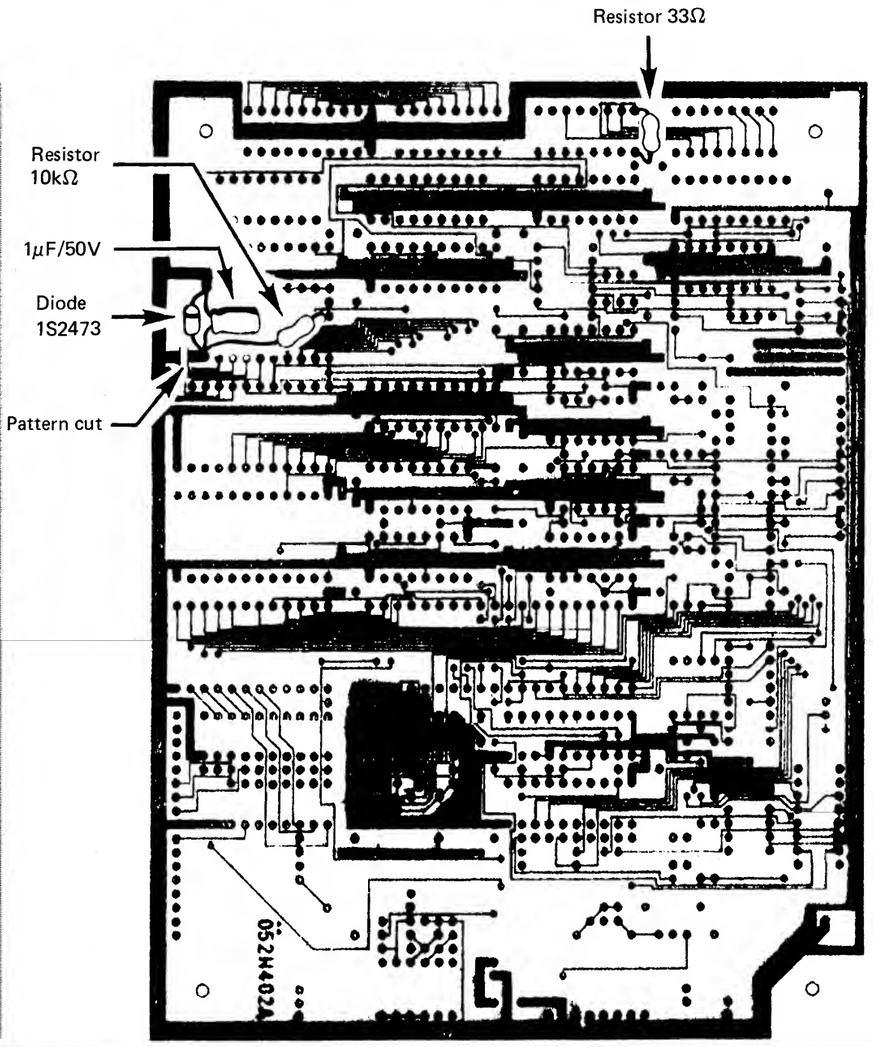
052H402B SERIAL NUMBER 280650-311799
Simillar to 052H402C except
some components are surface mounted.

MODIFICATION

For positive switch scanning in TAPE modes.
See detailed information in PANEL BOARD R Circuit Diagram.







View from foil side

This modification is unnecessary when TR3, R24, R25 and R26 are present on PANEL BOARD R.

R25J

Cearmic

Temperature Compensation Ceramic

Ceramic resonator CSA 12.00MX

Resistor array

Pin 1

2SC2603-E

2SA1115-E

emitter

Block-layer Ceramic

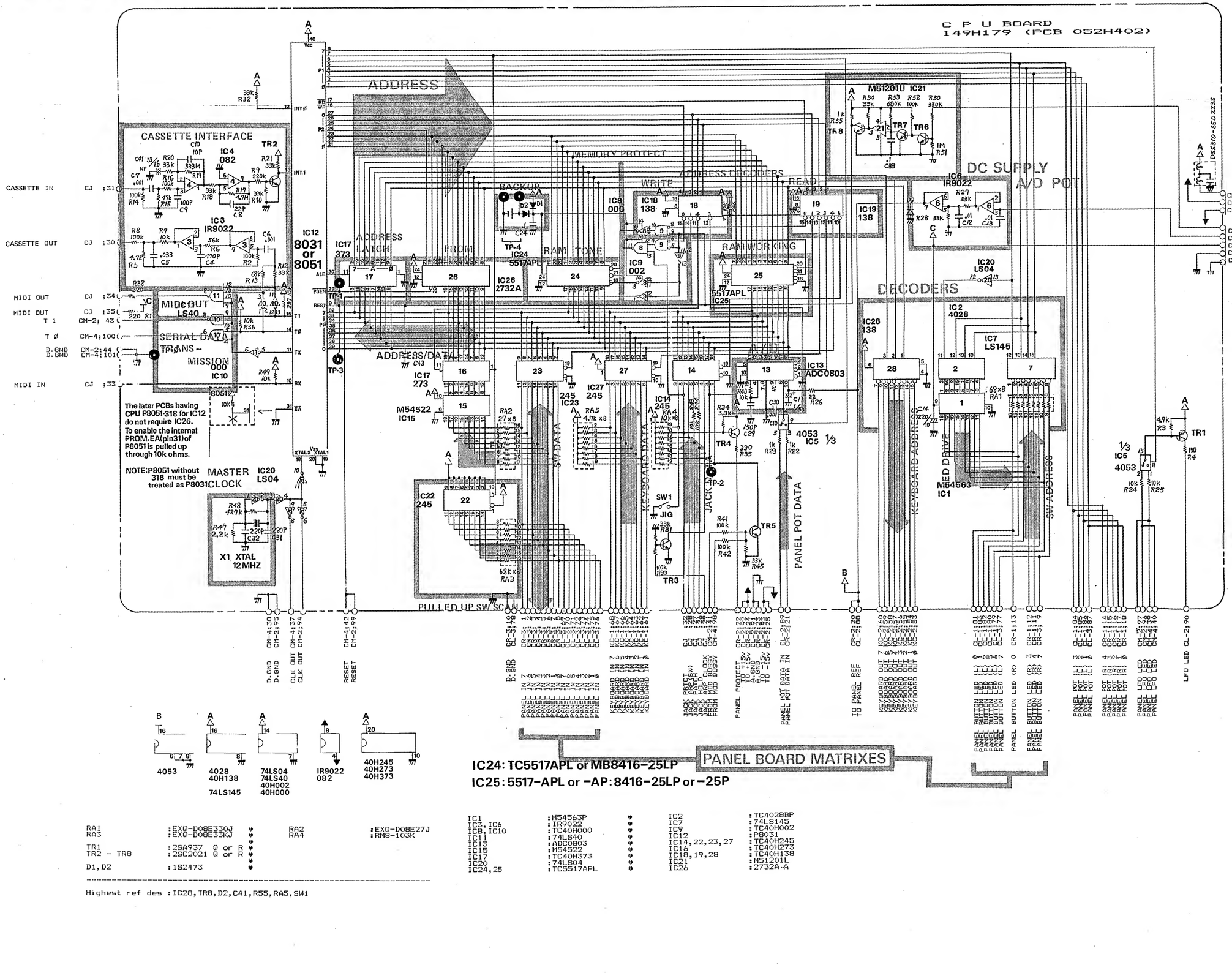
Mylar film

IS2473

EMI reduction Capacitor DSS310-55D223S

CIRCUIT DIAGRAM

CPU BOARD



RA1	:EXO-D08E330J	RA2	:EXO-D08E27J	
RA3	:EXO-D08E33KJ	RA4	:RM8-103K	
TR1	:2SA937 Q or R			
TR2 - TR8	:2SC2021 Q or R			
D1,D2	:1S2473			

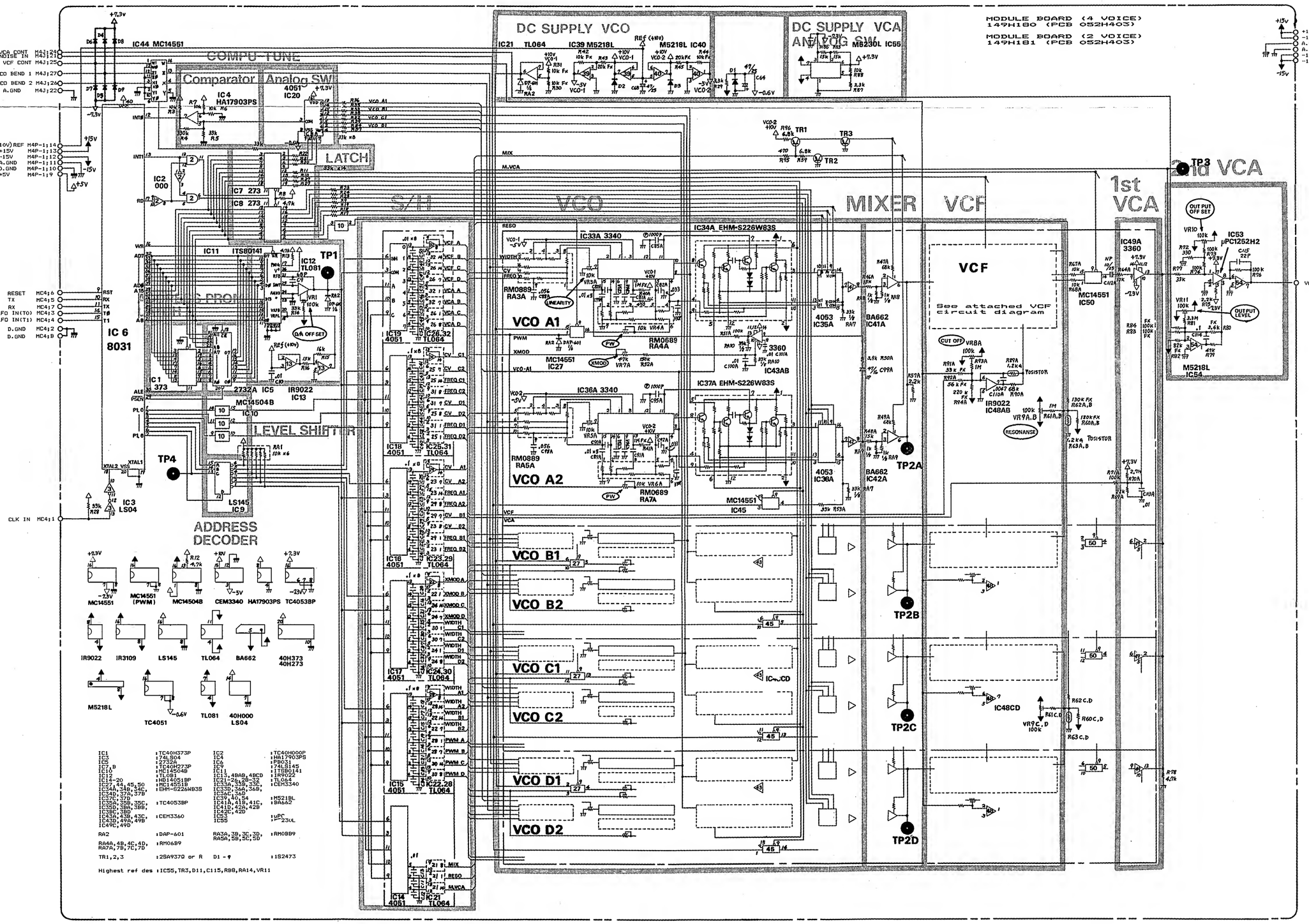
IC1	:M54563P	IC2	:TC4028BP	
IC3, IC6	:IR9022	IC7	:74LS145	
IC8, IC10	:TC40H000	IC9	:TC40H002	
IC11	:74LS40	IC12	:P8031	
IC13	:ADC0803	IC14,22,23,27	:TC40H245	
IC15	:M54522	IC16	:TC40H273	
IC17	:TC40H373	IC18,19,28	:TC40H138	
IC20	:74LS04	IC21	:M51201L	
IC24,25	:TC5517APL	IC26	:2732A-4	

Highest ref des :IC28,TR8,D2,C41,R55,RA5,SW1

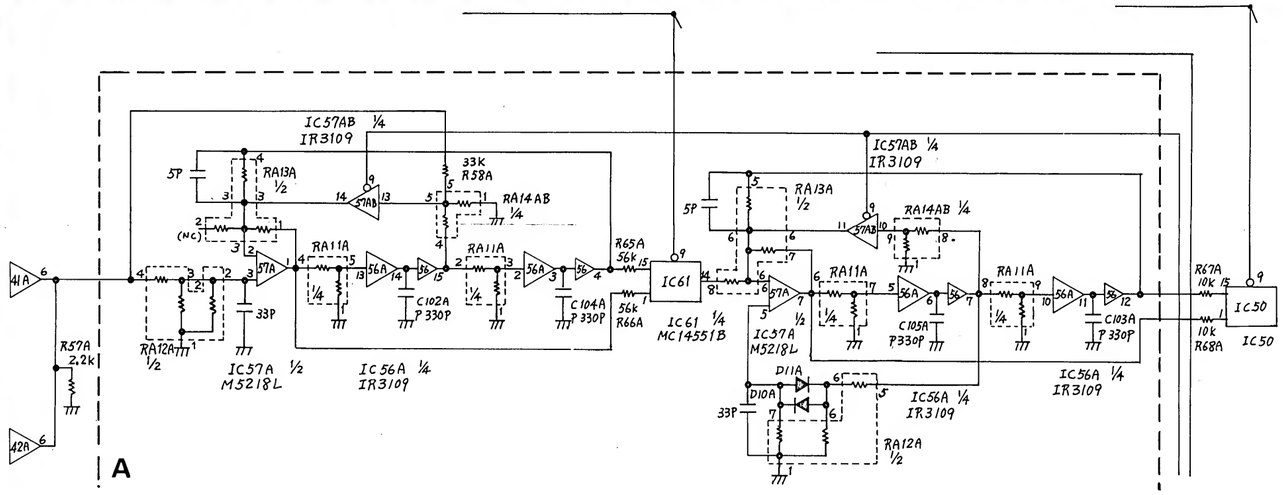
CIRCUIT DIAGRAM

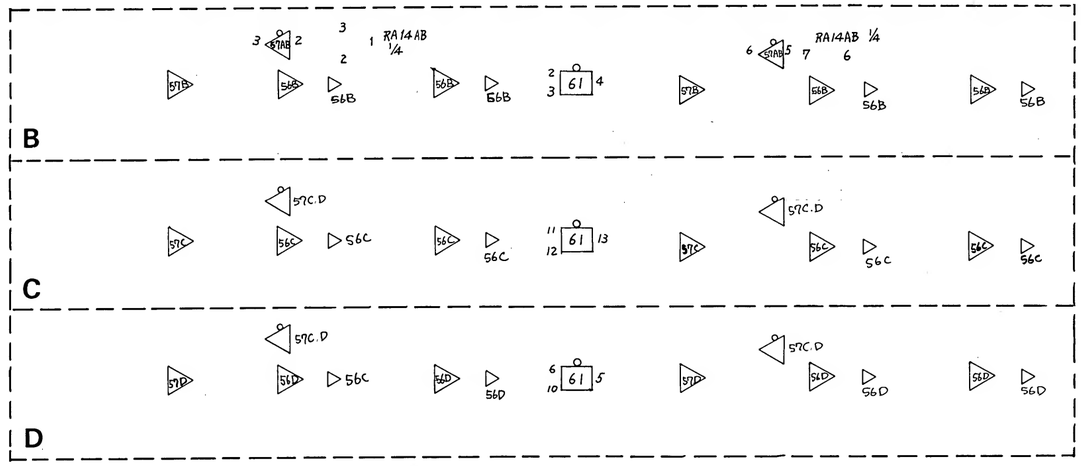
MODULE BOARD

SN up to 270649

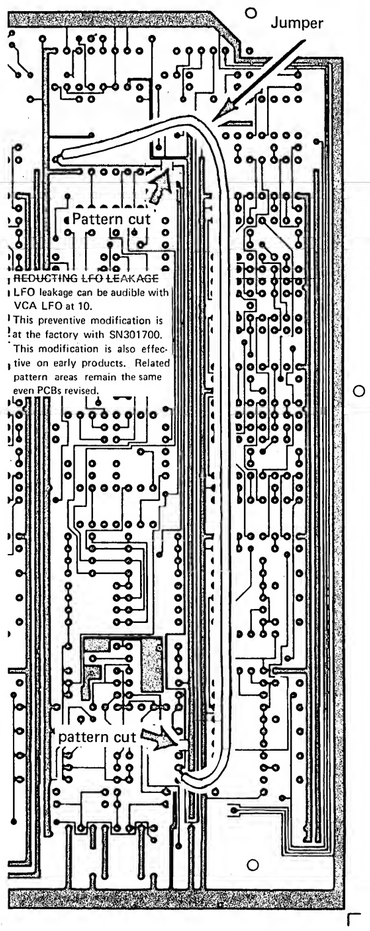


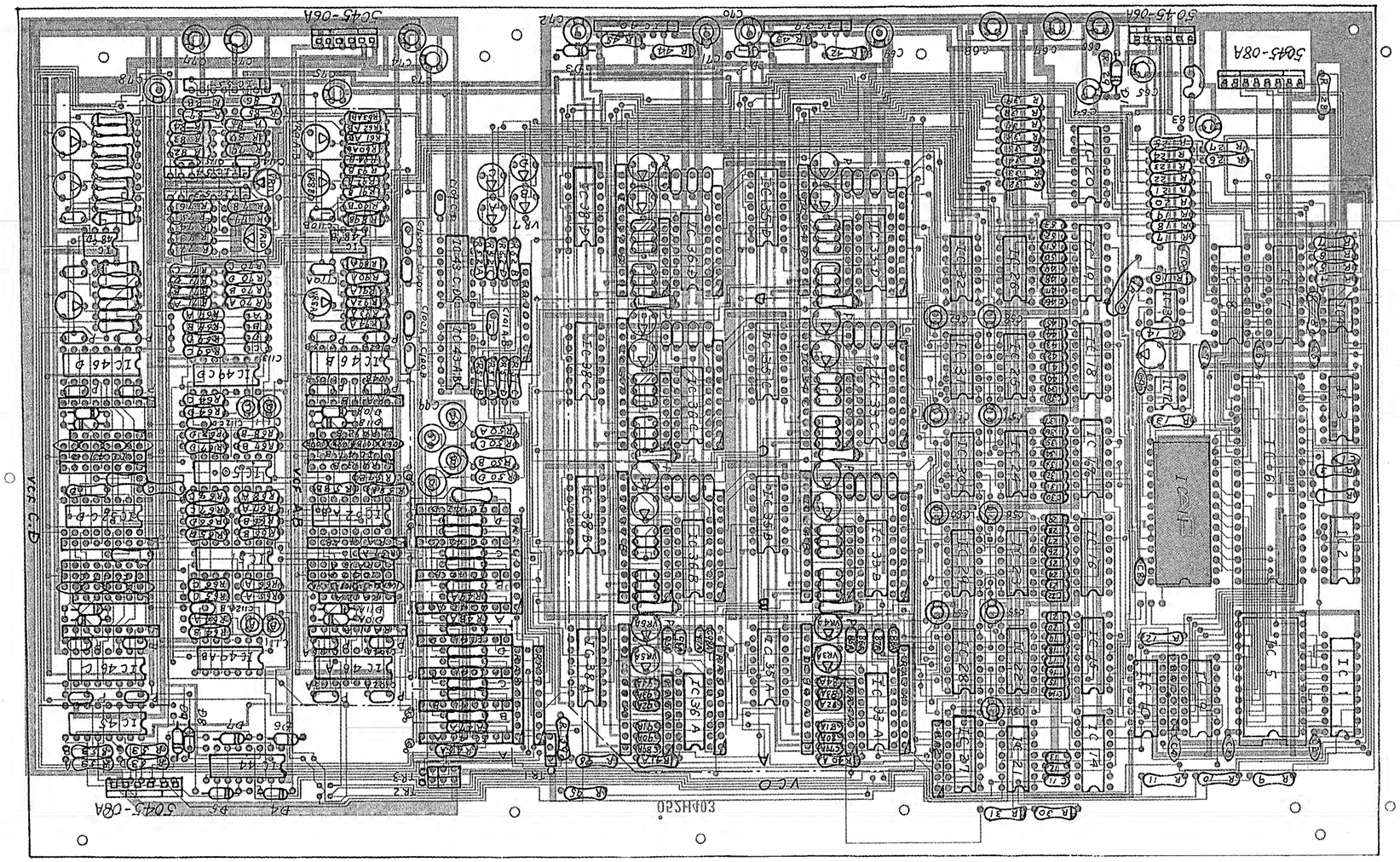
VCF CIRCUIT (detail)





The diagrams on the facing and this pages are not keyed to designations on PCB 052H403 but are to the layout below.





SERIAL NUMBER
UP TO 270649

MODULE BOARD

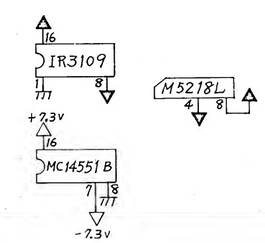
4-VOICE (149H180)
2-VOICE (149H181)
(pcb 052H403)

IMPROVING S/N RATIO
SN 290950–UP

R77	560	→ 1.8K
R80	2.2K	→ 3.3K
R81	100K	→ 22K
R82	33K	→ 6.8K
R83	4.7K	→ 10K
C117	22P	→ 150P

If conducting this modification on the unit SN280949 and below, proceed to 2. DC BAL in the adjustment section.

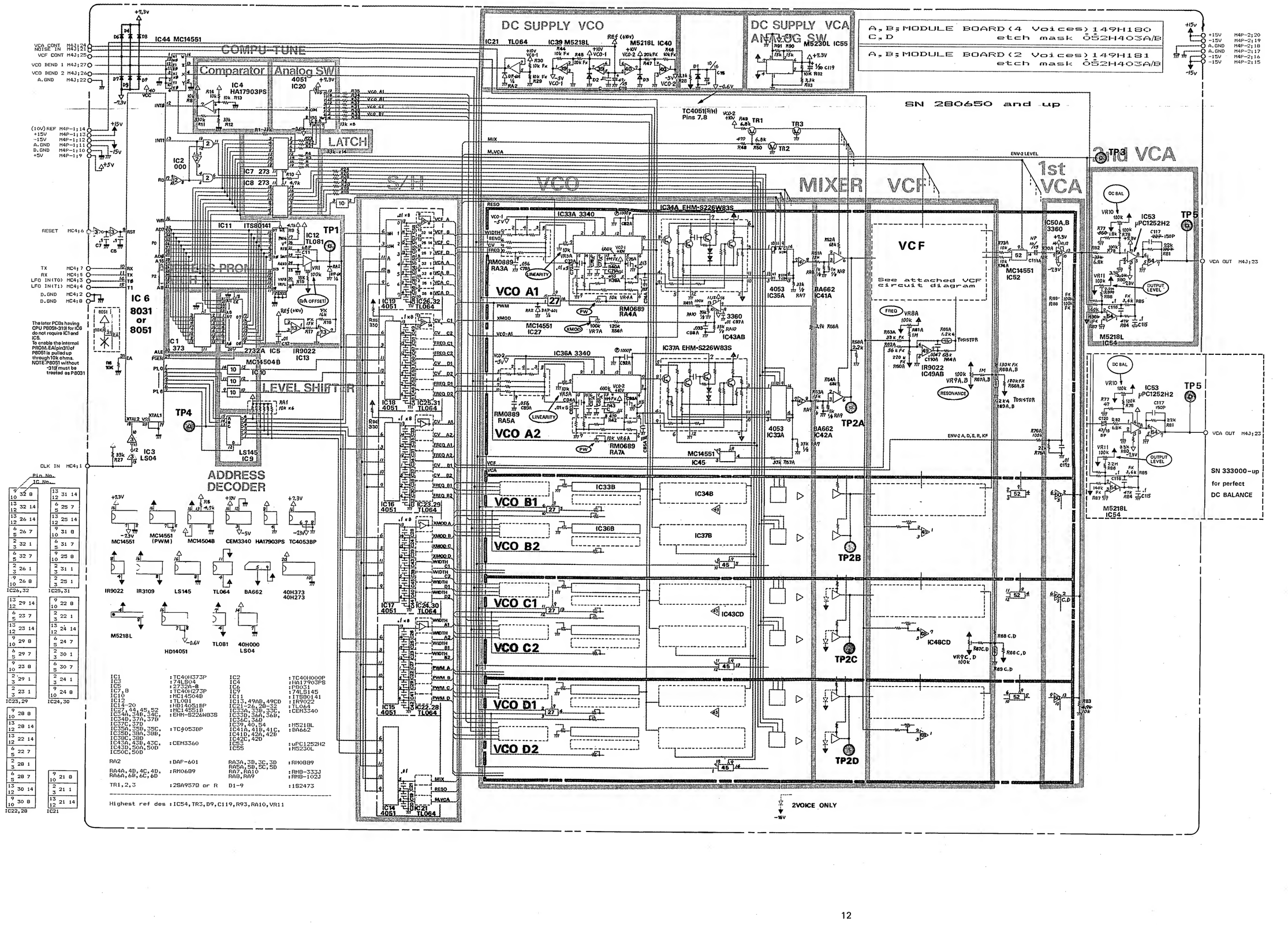
IC61	;	MC14551B
IC56A-56D, 57AB, 57CD	;	IR3109
IC57A-57D	;	M5218L
RA11A-11D, 14AB, 14CD	;	RM0891
RA12A-12D	;	RM0690
RA13A-13D	;	RM0688
D10, 11	;	1S2473



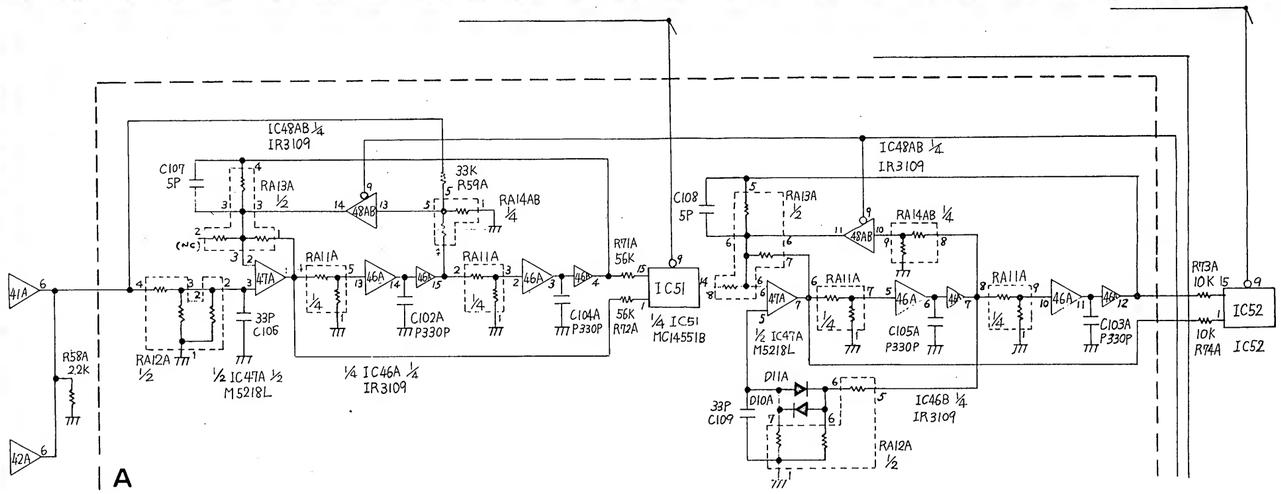
CIRCUIT DIAGRAM

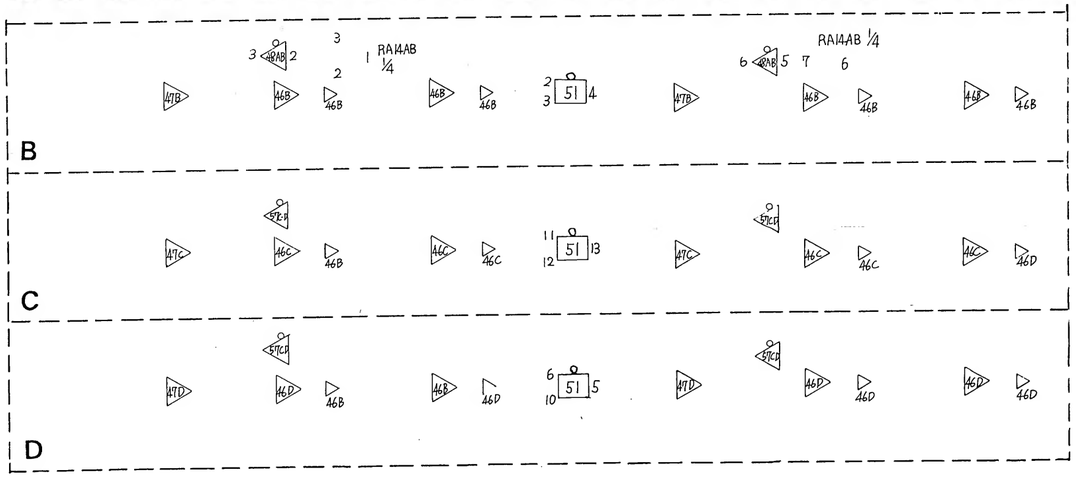
MODULE BOARD

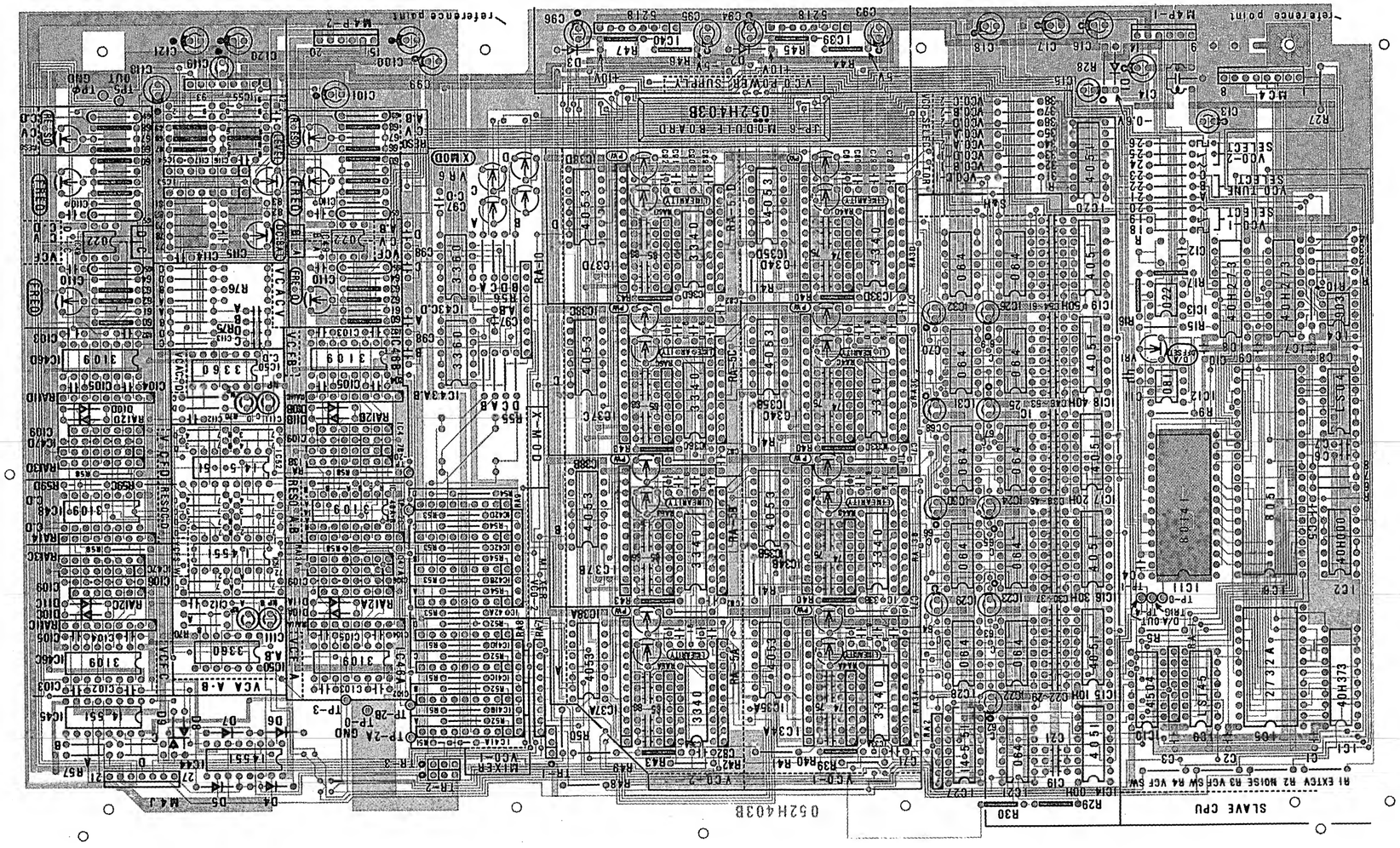
SN 280650 and up



VCF CIRCUIT (detail)







SERIAL NUMBER 311800 AND UP

MODULE BOARD

4-VOICE (149H180B)

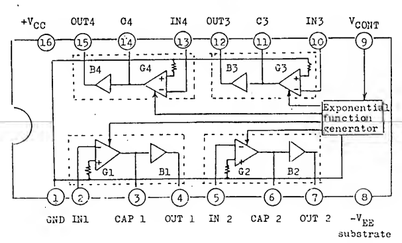
2-VOICE (149H181B)

(pcb 052H403B)

SERIAL NUMBER 280650-311799
(pcb 052H403A)

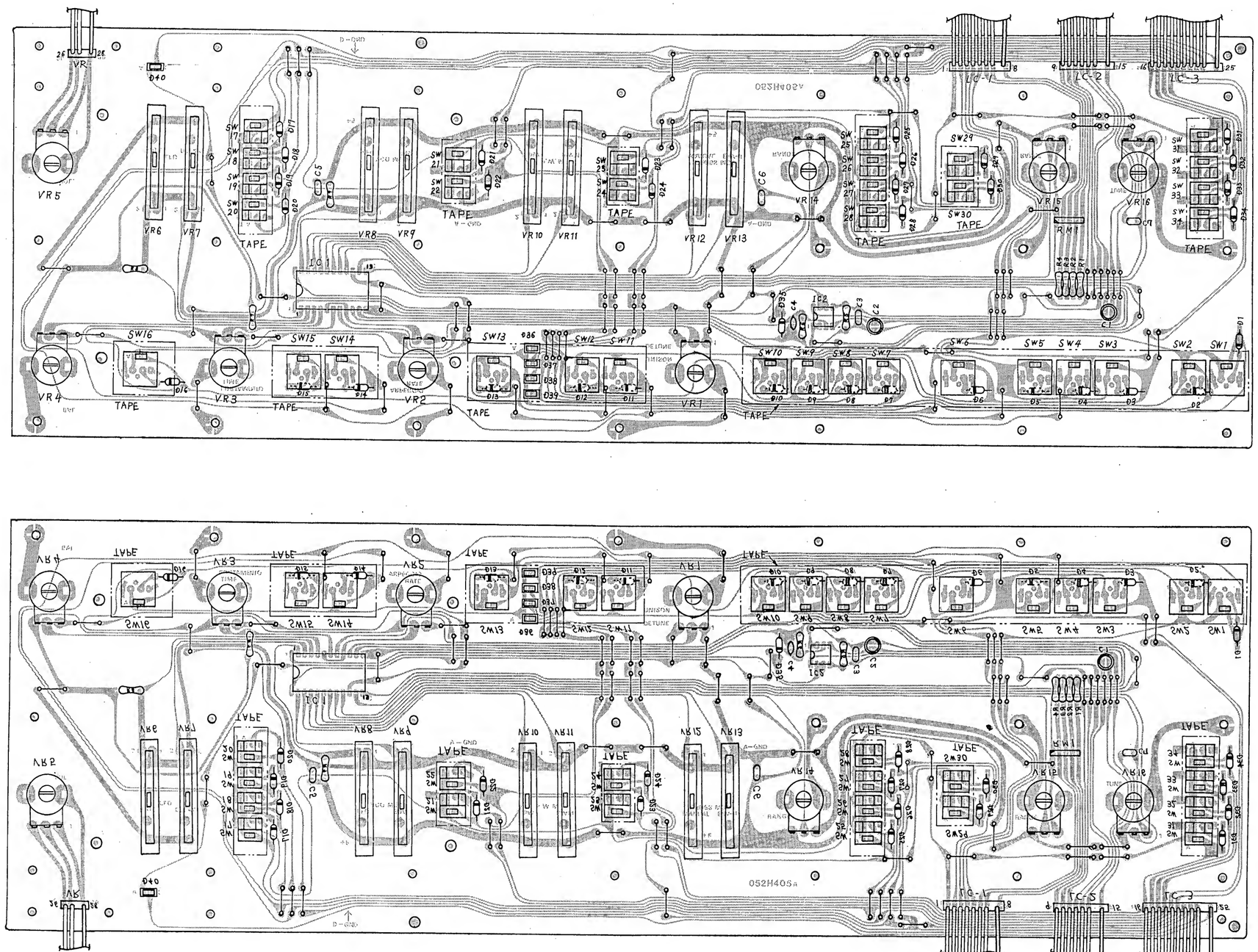
Similar to vertion B except some components are surface mounted on the foil side.

IR3109
(top view).

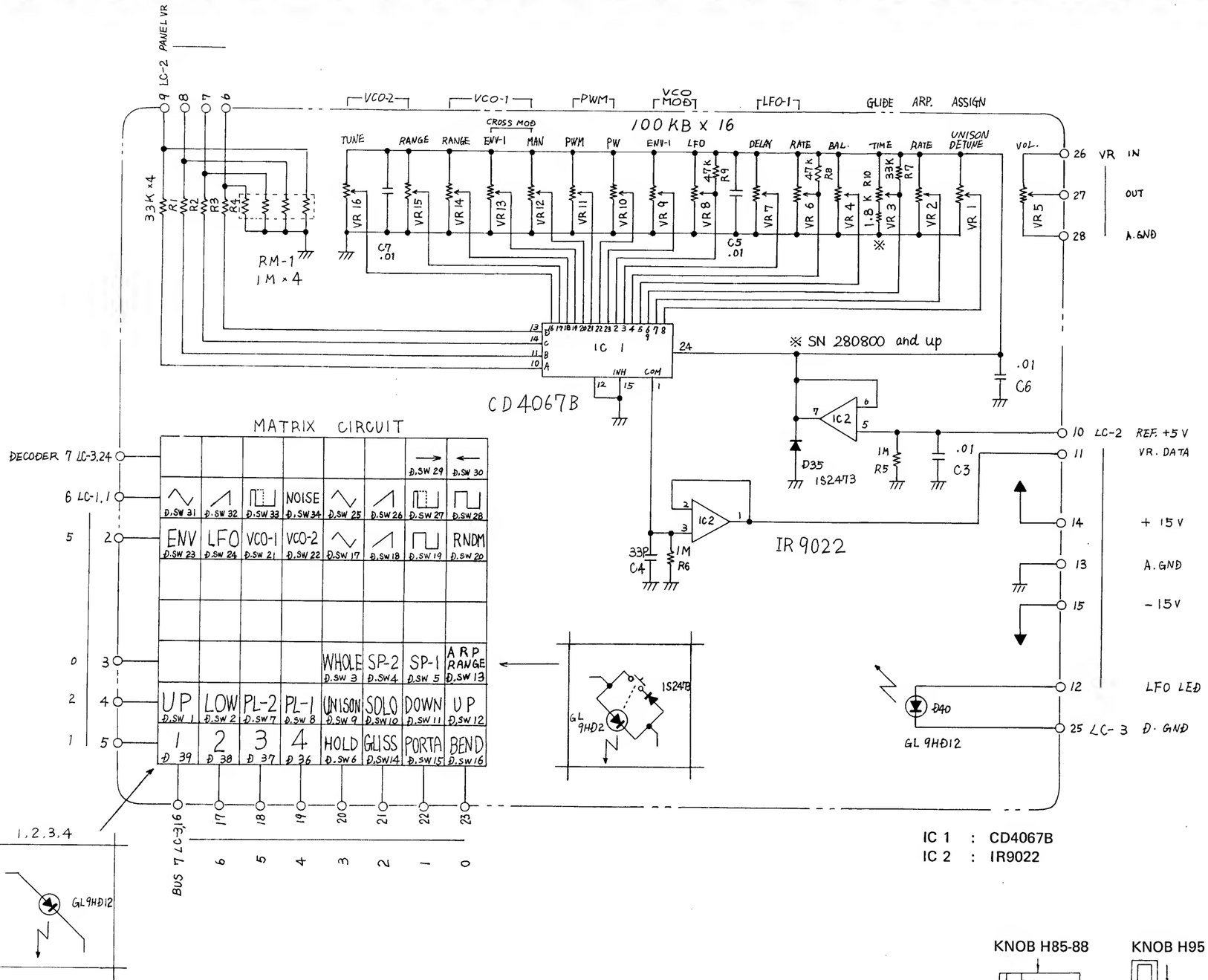


IC51	;	MC14551B
IC46A-46D, 48AB, 48CD	;	IR3109
IC47A-47D	;	M5218L
RA11A-11D, 14AB, 14CD	;	RM0891
RA12A-12D	;	RM0690
RA13A-13D	;	RM0688
D10, 11	;	1S2473

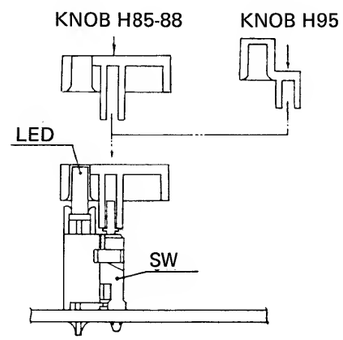
PANEL(L)BOARD (149H183A) (pcb 052H405A)



View from foil side



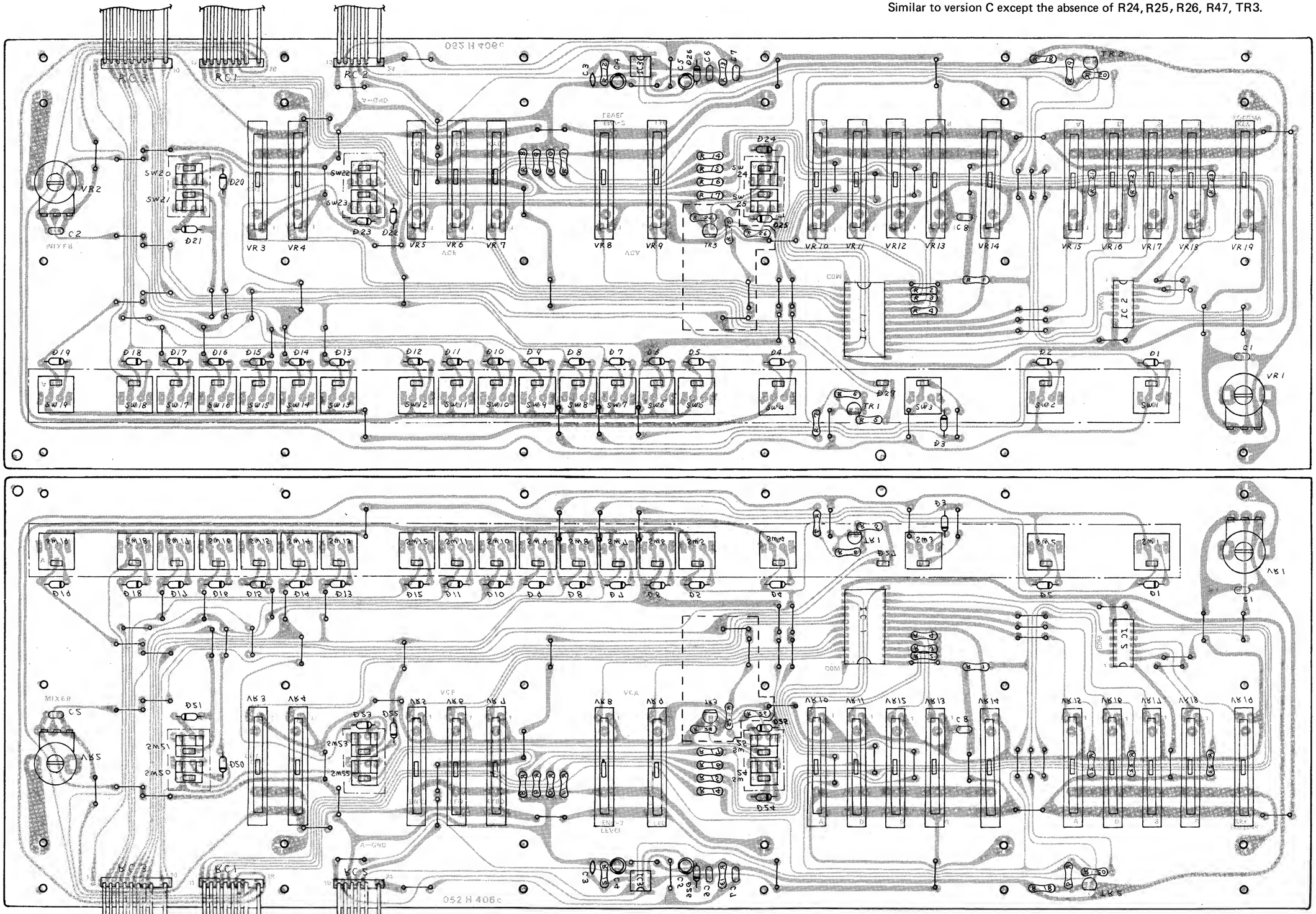
IC 1 : CD4067B
IC 2 : IR9022



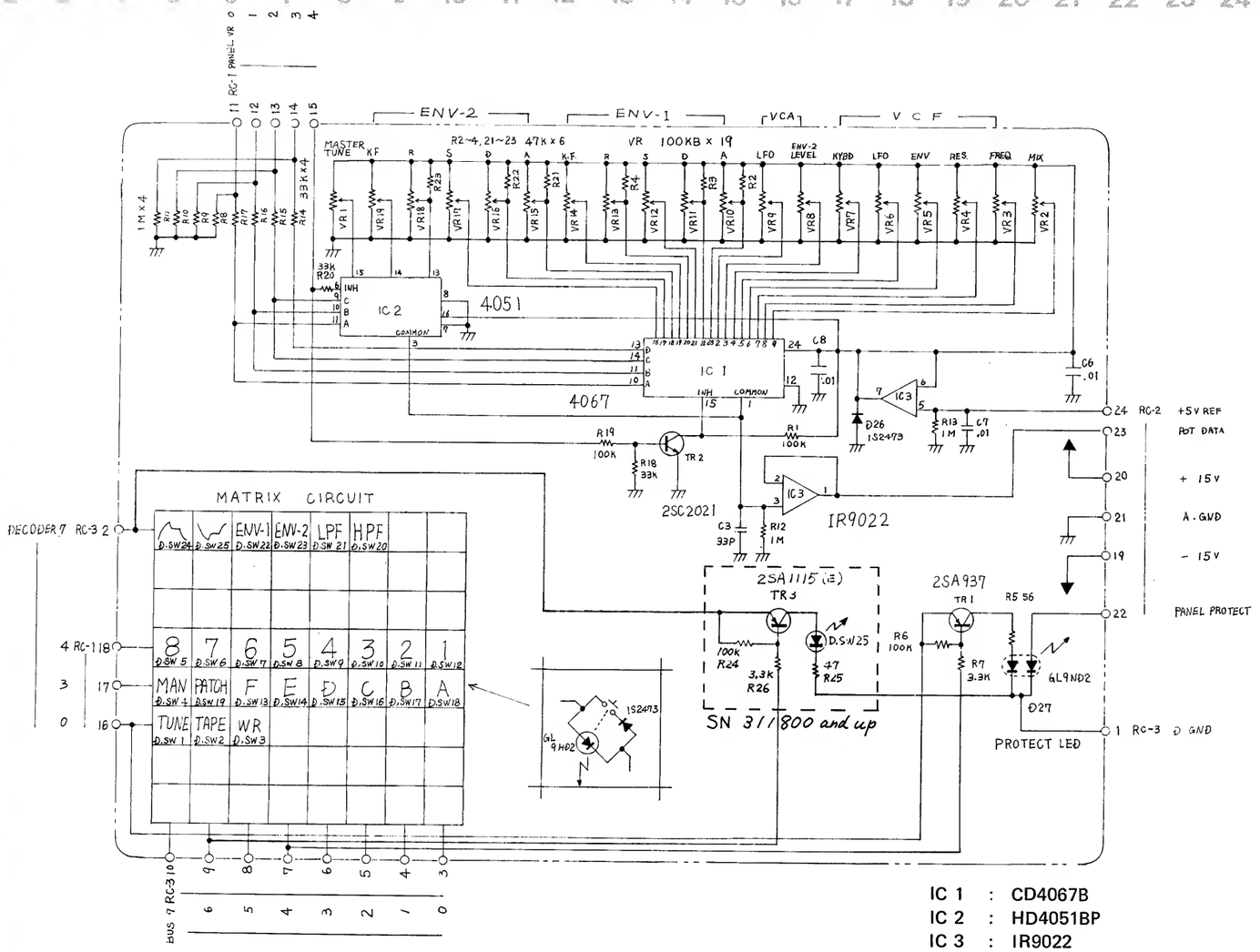
SERIAL NUMBER 31180 AND UP

PANEL(R)BOARD (149H184C) (pcb 052H406C)

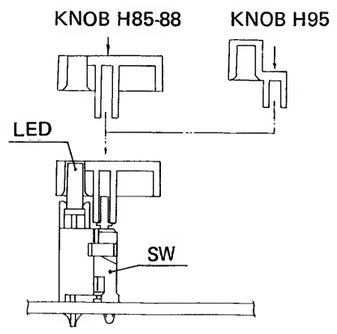
SERIAL NUMBER 250100-311799 (pcb 052H406B)
Similar to version C except the absence of R24, R25, R26, R47, TR3.



View from foil side



IC 1 : CD4067B
IC 2 : HD4051BP
IC 3 : IR9022



IMPROPER SWITCH SCANNING IN THE TAPE MODES

In early JP–6 the program in either "SAVE" "VERIFY" or "LOAD" sequence sometimes cannot escape the mode even when TAPE is pressed for canceling TAPE mode. This is due to the fact that TAPE contact is not sensed by the switch scanning. To cure this problem the factory modifies the circuitry by adding TR3, R24–R26 on the Panel board R as shown in the diagram.

For the products SN prior to 311800, an alternative modification shown in CPU BOARD layout should be conducted for easier retorfit.

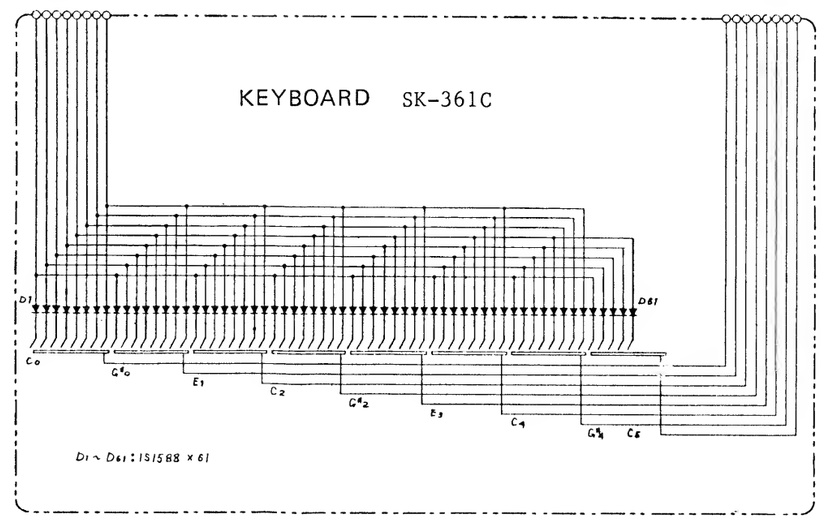
Remember that replacing CPU IC12 (CPU board) P8031 or P8051, with P8051-318 version does not cure the problem.

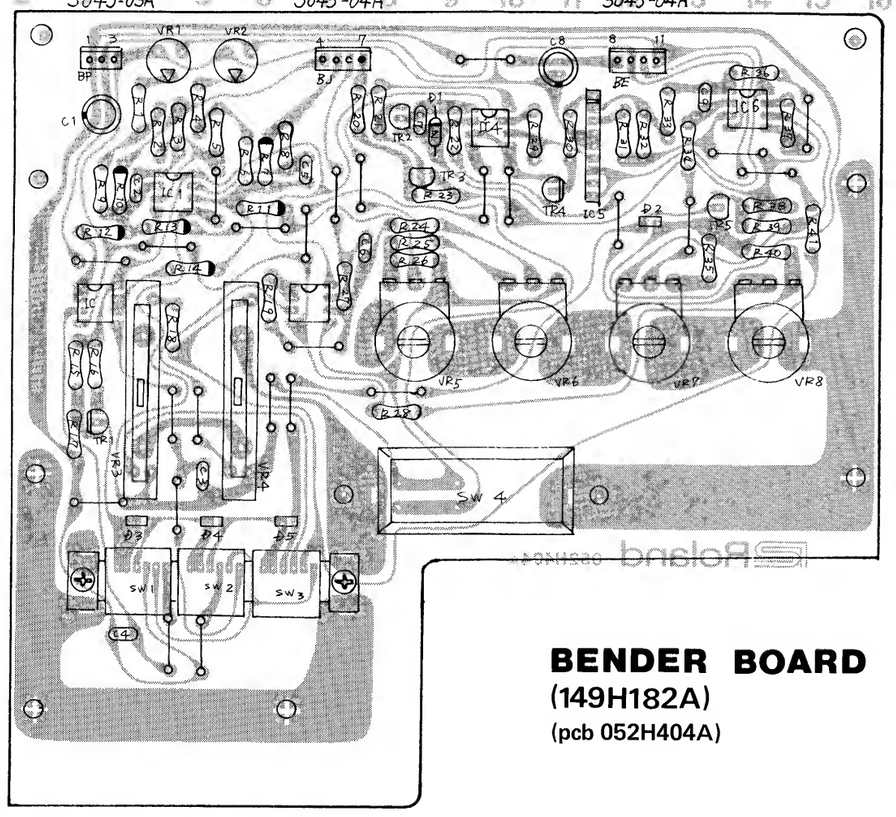
CPU BOARD

KC-1
0 61
1 62
2 63
3 64
4 65
5 66
6 67
7 68

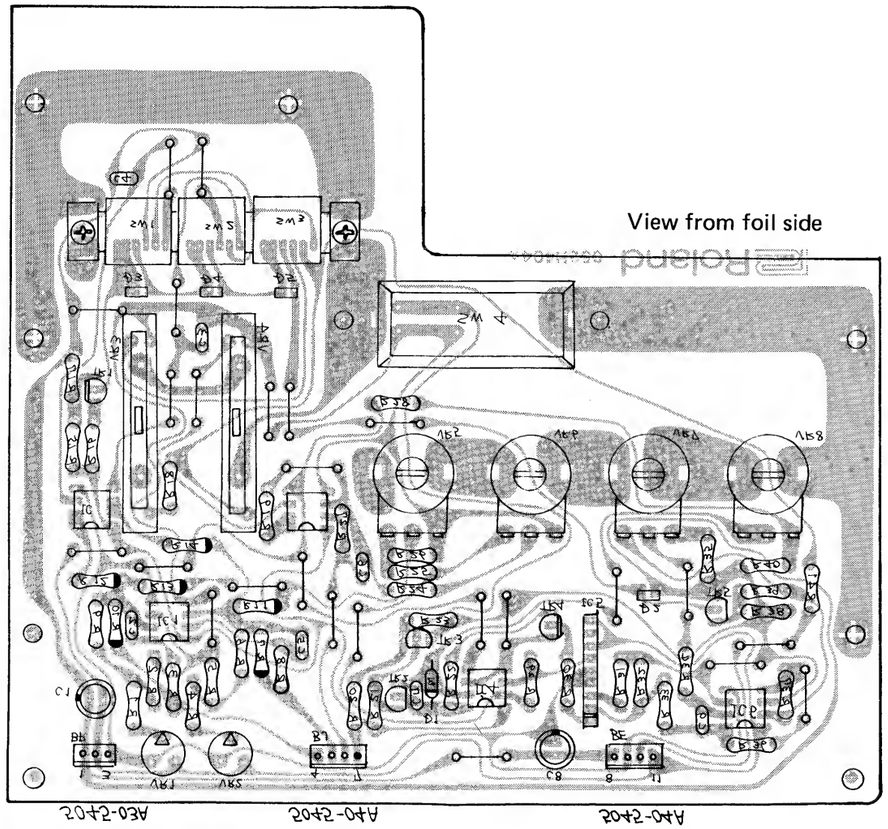
CPU BOARD

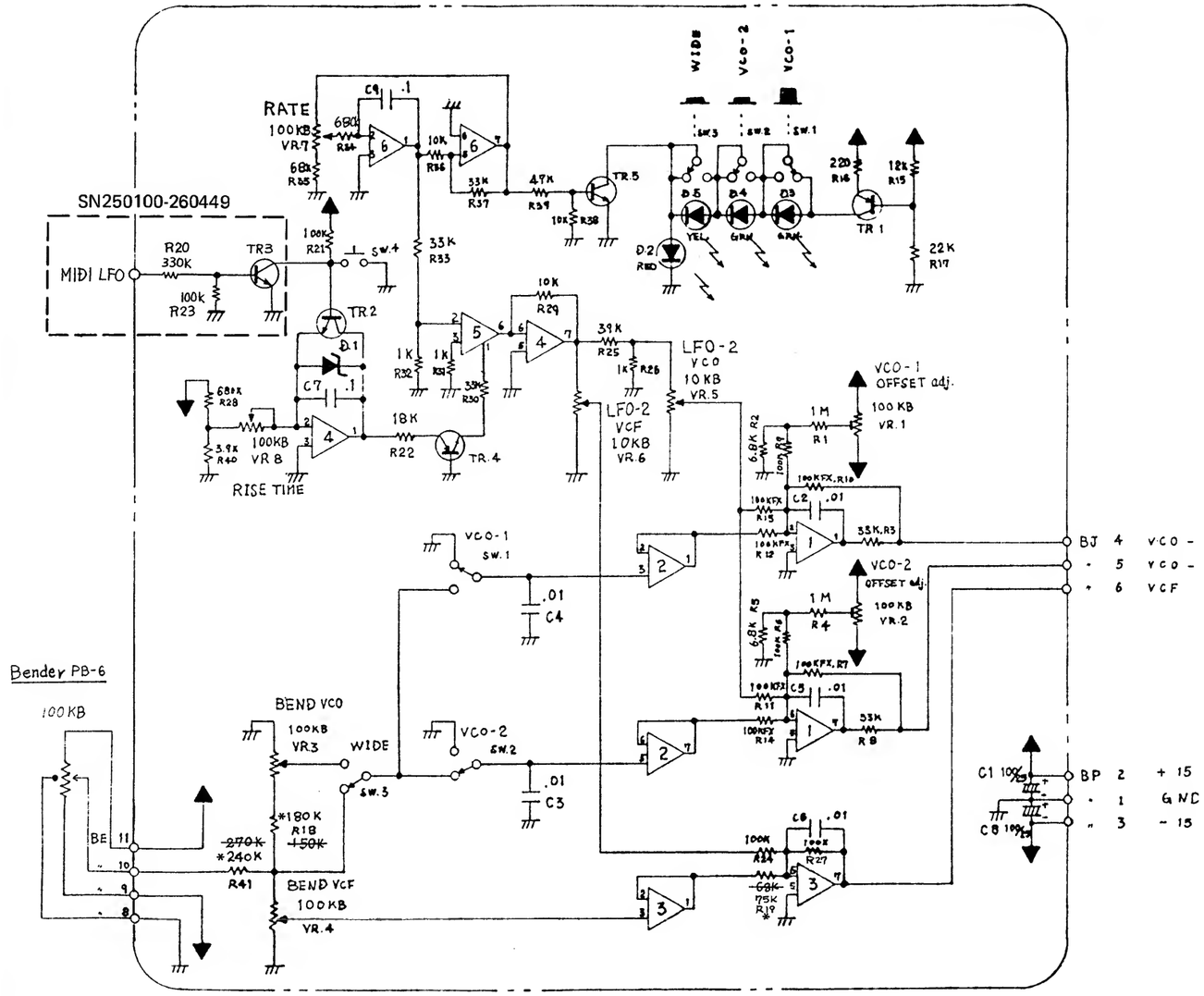
KC-2
0 53
1 54
2 55
3 56
4 57
5 58
6 59
7 60





BENDER BOARD
(149H182A)
(pcb 052H404A)





* SN280850 and up

VR3,VR4 ——
S3018P405-B15 (100KB)

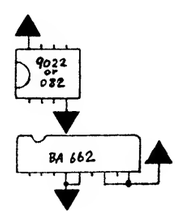
VR7,VR8 ——
EVH5XAB15 B15 (100KB)

VR5,VR6 ——
EXV5XAB15 B14 (10KB)

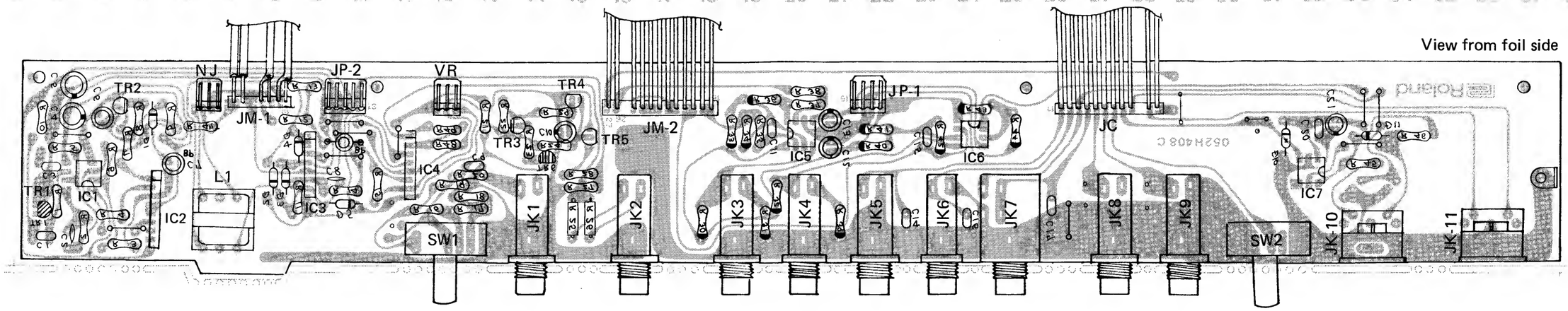
SW4 —KEH10003 (Ass'y)
SW1,SW2,SW3 ——
SUT32A-4 (Ass'y)

UNLESS OTHERWISE SPECIFIED
ALL PNP TRANSISTORS ARE 2SA937-Q or 2SA1115-E
ALL NPN TRANSISTORS ARE 2SC2021-Q or 2SC2603-E

IC 1,4,6	:	IR9022
IC 2,3	:	082
IC 5	:	BA662
D 1	:	05Z11X



View from foil side

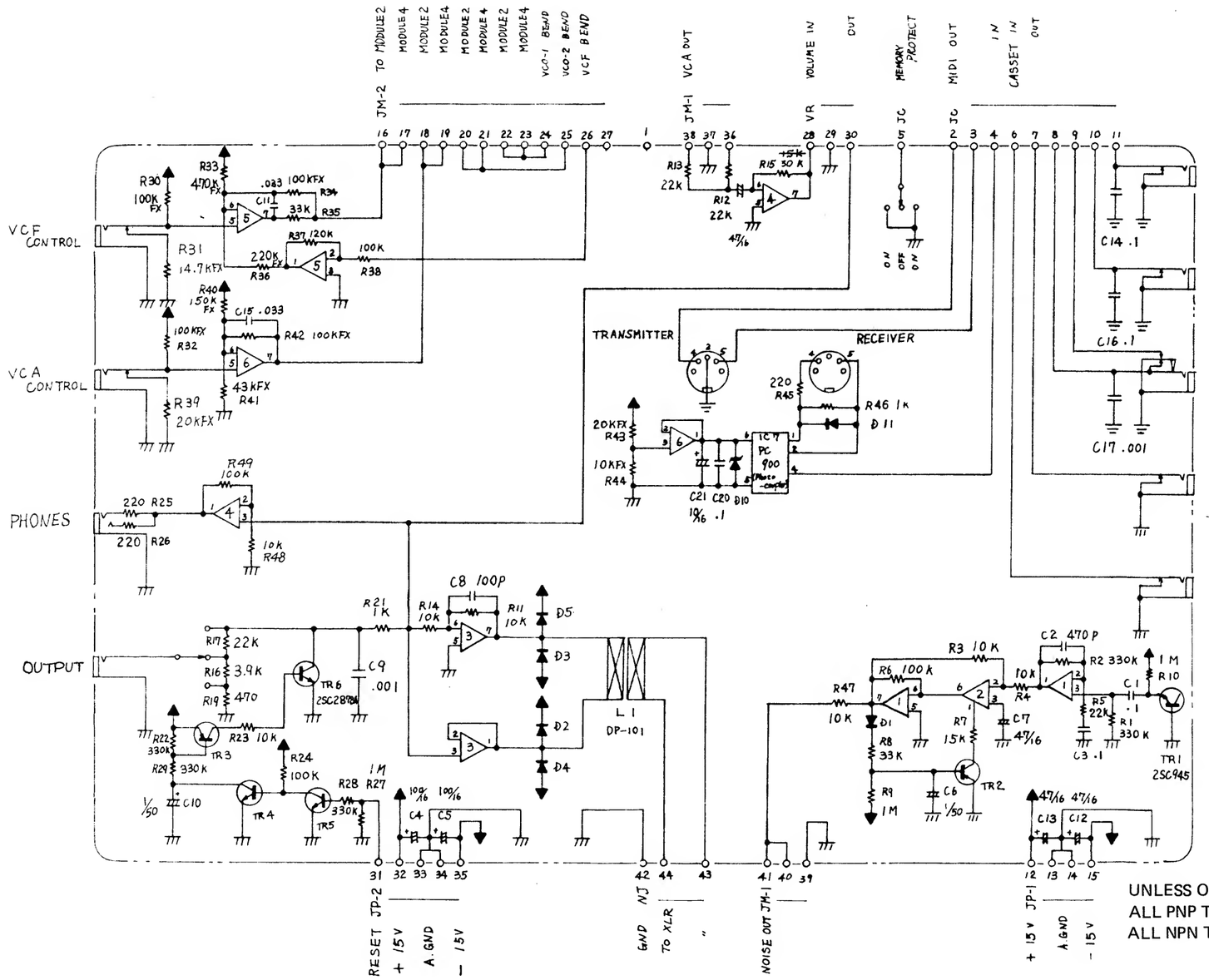


JACK BOARD

(149H186C)

(pcb 052H408C)

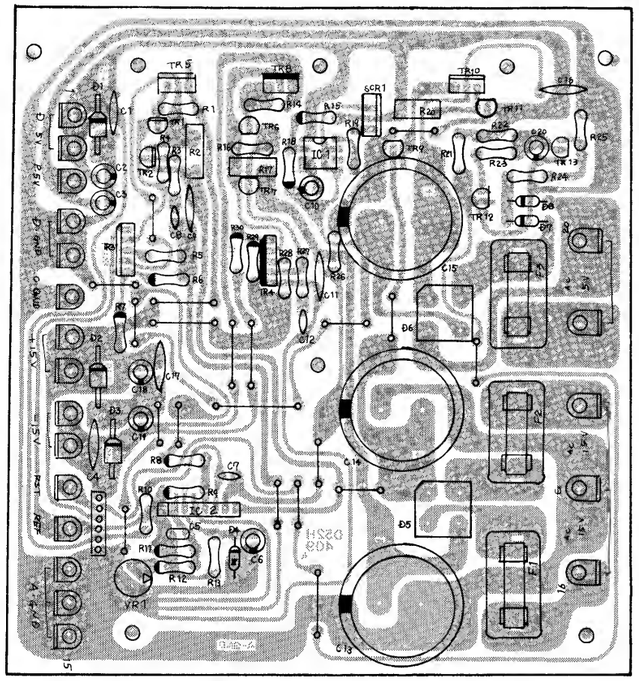
INCREASING OUTPUT LEVEL
SN 290950–UP
Changing R15 across IC4 pins from 15k to 30k doubles signal amplitude at OUTPUT and PHONES jacks.



2SA937
2SC2021
R-25J
CRB25FX
Mylar film cap
Ceramic disc cap
1S2473
Zener 05Z6.2
R50J
Electrolytic
Jumper

IC 1,6 : IR9022
IC 5 : μPC4558
IC 2 : BA662
IC 3,4 : M521BL
D 10 : 0.5Z6.2

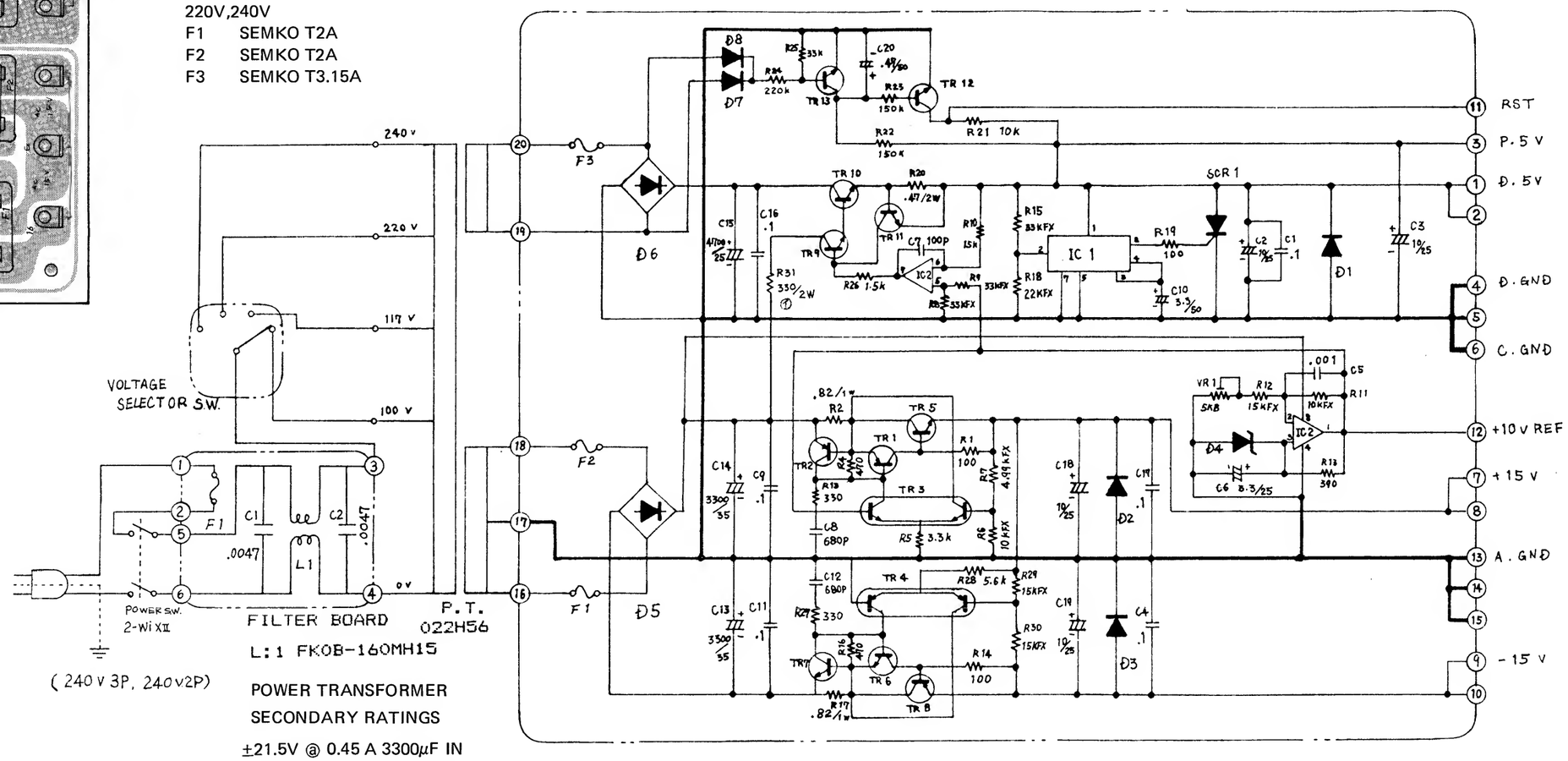
UNLESS OTHERWISE SPECIFIED
ALL PNP TRANSISTORS ARE 2SA937-Q or 2SA1115-E
ALL NPN TRANSISTORS ARE 2SC2021-Q or 2SC2603-E



POWER SUPPLY BOARD
(162H061A) 100/117V
(162H062A) 220/240V
(pcb 052H409A)

100V,117V
F1 T-GGS2 (CSA) 2A
F2 T-GGS2 (CSA) 2A
F3 T-GGS3.15 (CSA) 3.15A

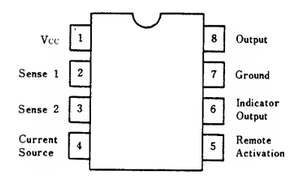
220V,240V
F1 SEMKO T2A
F2 SEMKO T2A
F3 SEMKO T3.15A



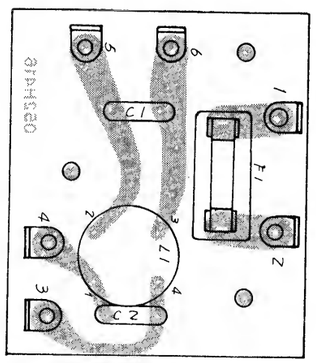
IC 1	: μPC3423C		SCR 1	: 5P05M	
IC 2	: M5218L		D 4	: 1SZ59	
TR 5,10	: 2SD1406		D 5, 6	: 2B4B41	
TR 8	: 2SB1015		D 1, 2, 3	: Hi–Fi SPECIAL	
TR 3	: 2SC1583		D 7, 8	: 1S2473	
TR 4	: 2SA798				

UNLESS OTHERWISE SPECIFIED
ALL NPN TRANSISTORS ARE 2SC2021-Q or 2SC2603-E
ALL PNP TRANSISTORS ARE 2SA937-Q or 2SA1115-E

μPC3423C
Pin Configuration



FILTER BOARD
(149H191) 100/117V
(149H192) 220/240V
(pcb 052H416)



100V,117V
F1 T-GGS1 (CSA) 1A

220V,240V
F1 SEMKO T3.15mA

MAINTENANCE AND ADJUSTMENT

Reading through "PROGRAM FUNCTION" and "WHAT ADJUSTED" in MODULE BOARD ADJUSTMENT section and "MODULE CONTROL VOLTAGES" in the Circuit Description will help in understanding the JP-6 performance, in troubleshooting as well as in understanding adjustment theory. In maintaining the JP-6 observe the following cautions.

CAUTIONS:

When the JP-6 program cannot proceed orderly or overruns intermittently, first check the power line for excessive fluctuation, loose contact or external pulses.

When Patch Memories are volatile, check power-backup circuitry (CPU board–diodes D1 and D2 and the battery).

NOTE: Nominal battery voltage ..... 3V.
Minimum backup voltage .... 2V.
Battery voltage must be more than 2.6V.

IC24 RAM SHOULD BE TC5517APL or MB8416-25LP (low current consumption) for the longer battery life expectancy.

When the program can not escape the TAPE modes, see Panel Board R Circuit diagram for modification.

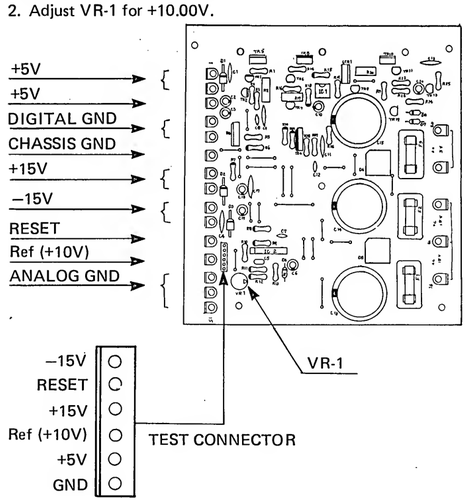
Saving the Patch memories on tape before starting troubleshooting is recommended to prevent the possible volatilization.

ADJUSTMENT

Check and readjust DC supply (as necessary) before starting particular adjustment.

POWER SUPPLY BOARD

1. Connect the digital voltmeter to Ref (+10V) terminal.
2. Adjust VR-1 for +10.00V.



3. Confirm the remaining terminal voltages. They must be:

+5V ± 30mV
+15V ± 100mV
–15V ± 400mV

The JP-6 contains the adjustment program to provide specific parameters for individual adjustment which can be evoked through BANK and NUMBER buttons when the JP-6 is in the TEST mode. To put the unit into the TEST mode, first turn the power ON, then place SW-1 (DIP SW) of the CPU board at JIG position.

CAUTION:
* Setting SW-1 before power up does not turn the JP-6 to the TEST mode.

MODULE BOARD

Refer to ADJUSTMENT LOCATIONS at the end of this section for the locations of TEST POINTs and TRIMMERs.

CAUTION:
* Adjustment Order:
Each of the following two groups is considered as an adjustment unit (set) and must be conducted in the order numbered.

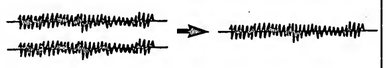
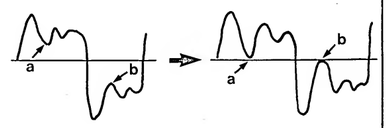
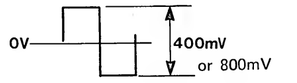
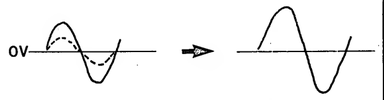
A1 and A2 A4, A5 and A6

Other adjustments are independent of each other.
Be sure to turn SW-1 off after completion of the adjustment(s).

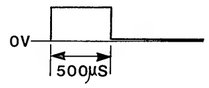
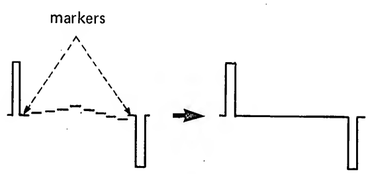
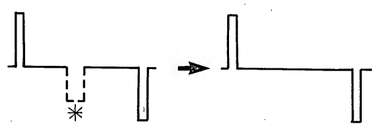
COMMON SETTINGS TO ALL THE FOLLOWING ADJUSTMENTS

VOLUME: 10
OUTPUT LEVEL (Rear Panel): H
KEY MODE: SPLIT-1 or SPLIT-2
PANEL MODE: LOWER-4 Voice MODULE BOARD
or UPPER-2 Voice MODULE BOARD
BANK and NUMBER: As stated in an adjustment.
OSCILLOSCOPE: SLOPE (TRIGGER) "+",
(otherwise stated) PROBE 1 : 1

Example: LINEARITY
Press SPLIT-1 or SPLIT-2. Press UPPER. Press BANK D and NUMBER (example 1 = VCO A1 of 2 VOICE MODULE). If successively adjust 4 VOICE MODULE, press LOWER. LEDs D and 1 change to A-1. Press D and a NUMBER again.

PANEL SETTINGS	ADJUST	PROGRAM FUNCTION	WHAT ADJUSTED/
1. D/A			
1-1. OFFSET			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **A-1**	1. Connect digital voltmeter between TP-1 and TP-0 (GND) (on MOD PCB). 2. Adjust VR1 (D/A OFFSET) for 0V ± 0.1mV.	Set the input bits to the D/A Converter (IC11 of the CPU Board) to 0.	The offset of the operational amplifier (IC12).
1-2. Checking D/A converter			
UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **A-2**	After setting BANK/NUMBER, see if TUNE LED of the panel goes out within 2-3 seconds. If not, repeat steps in 1-1, (adjust D/A OFFSET VR1).	Connect D/A outputs of various voltages to VCO A-1 and measure its corresponding output sequences.	If the TUNE LED remains lit for more than several seconds, check D/A, VCO A-1 and A-2.
2. DC BAL			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **A-3** OSCILLOSCOPE H: 0.1ms/cm V: 5mv/cm AC Coupling	1. Connect the scope to OUTPUT JACK or R21 (JACK BOARD). 2. Adjust VR10 (DC BAL) for the minimized DC drift. Increase scope sensitivity as necessary. 	Apply LFO output (square, between 0V and +10V) to the final VCA IC53.	The offset of the VCA.
3. RESONANCE			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **A-4 (VR9AB)** **A-5 (VR9CD)** OSCILLOSCOPE H: 0.1ms/cm V: 200mV/cm AC Coupling	1. Connect the scope to OUTPUT JACK or R21 (JACK BOARD). 2. Adjust VR9 (RESO) so that a and b in Fig. 2 are positioned to the 0V line. 	Apply VCO output, together with RESONANCE and CUTOFF data, to two VCFs.	Amount of feedback for a proper regeneration.
4. OUTPUT LEVEL			
PANEL MODE UPPER (2VOICE) LOWER (4 VOICE) BANK/NUMBER **A-6**	1. Connect the scope to OUTPUT JACK. 2. Adjust VR-11 (LEVEL) for 400mVp-p (SN up to 280949) or 800mVp-p (SN 290950-up) as shown below. 	Apply the predetermined control voltages and input signal to the final VCA IC53.	See JACK BOARD diagram for change information.
5. CUTOFF			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **B-1 (A)** **B-2 (B)** **B-3 (C)** **B-4 (D)** OSCILLOSCOPE H: 0.1ms/cm V: 500mV/cm AC Coupling	1. Connect the scope to OUTPUT JACK or R21 (JACK BOARD). 2. Adjust VR8 (CUTOFF or FREQ) for the maximum amplification. 	Feed square wave (of a predetermined frequency and level) from a VCO to the VCF while set the VCF to full resonance.	Tune the resonance frequency to that of the VCO.

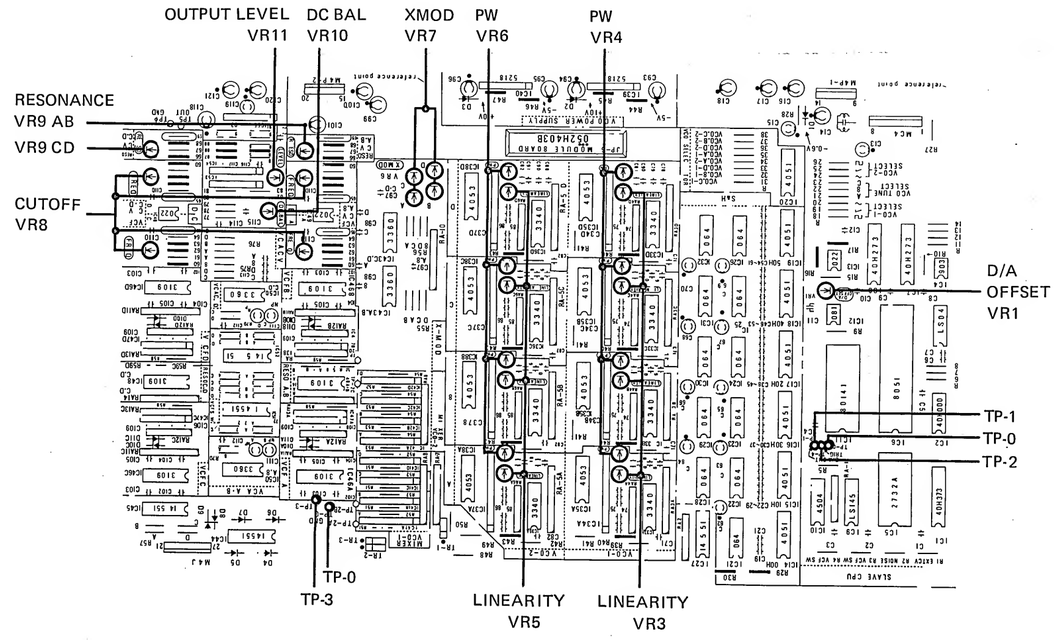
JUNE 13, 1983

PANEL SETTINGS	ADJUST	PROGRAM FUNCTION	WHAT ADJUSTED/ DESCRIPTION
6. PW			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **C-1 (VR4A)** **C-2 (VR6A)** **C-3 (VR4B)** **C-4 (VR6B)** **C-5 (VR4C)** **C-6 (VR6C)** **C-7 (VR4D)** **C-8 (VR6D)** OSCILLOSCOPE TRIG: MANUAL H: 0.1ms/cm V: 500mV/cm AC Coupling	1. Connect the scope to OUTPUT JACK or R21 (JACK BOARD). 2. Adjust VR4 (VR6) (PW) for the 500μs pulse length. 	Apply predetermined control voltages (frequency, PW) to the VCO.	Pulse width to the specified duty ratio.
7. LINEARITY			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **D-1 (VR3A)** **D-2 (VR5A)** **D-3 (VR3B)** **D-4 (VR5B)** **D-5 (VR3C)** **D-6 (VR5C)** **D-7 (VR3D)** **D-8 (VR5D)** OSCILLOSCOPE H: 0.1ms/cm V: 500mV/cm AC Coupling	1. Connect the scope between TP-3 and TP0 (GND). 2. Adjust VR3 (VR5 LINEARITY) for straightness by aligning signals to the markers. Increase V sensitivity for fine adjustment. Press the BANK/NUMBER button again when the detune is too great for adjustment. 	Enable Compu-Tune feature (for WIDTH and FREQ) upon pressing BANK/NUMBER, then apply control voltages to the VCO in 8 steps. Measuring the result frequency, present detune data at TP-3.	Linearity of VCO.
8. X MOD			
PANEL MODE UPPER (2 VOICE) LOWER (4 VOICE) BANK/NUMBER **E-1 (VR7A)** **E-2 (VR7B)** **E-3 (VR7C)** **E-4 (VR7D)** OSCILLOSCOPE H: 0.1ms/cm V: 500mV/cm AC Coupling	1. Connect the scope between TP-3 and TP0 (GND) of MOD BOARD. 2. Adjust VR7 (X MOD) for flattening the part (*) as shown in Fig. 7.  Note: The part can be a positive going pulse.	Synchronize the VCO-2 with the VCO-1, then apply the VCO-2 output (amount equal to that when CROSS MOD MANUAL is 5) to the VCO-1. Present at TP-3 the difference between an ideal and the actual VCO-1 output frequencies.	Prevention of unfavorable modulation signals.

BENDER BOARD

1.			
BANK/NUMBER **F-1 (VR1)** **F-2 (VR2)** OSCILLOSCPE H: 0.1ms/cm V: 500mV/cm AC Coupling	1. Connect the scope between TP-3 and TP-0 of either MOD BOARD. 2. Adjust VR1 (VR2) in the same manner as in 8. X MOD. The BENDER lever must be at the neutral position.	Present at TP-3 the difference between the frequencies from the VCO while placing a ground intermittently to the BEND IN of the VCO.	BENDER output to 0.

NOTE: Designations for extention-lines VRs and TPs shown below are applicable to all PCB revisions.
Some PCBs have wrong designation(s).



PARTS LIST

CHASSIS

061H147D	Chassis H147D
063H057	Side panel H57 (right)
063H058	Side panel H58 (left)
063H061	Plate H61 (Power transformer)
063H056A	Voltage selector plate H56A
061H149	Chassis H149 (JACK BOARD)

PANEL

072H142A	Top panel H142A
072H141	End block H140 (right)
072H140	End block H141 (left)

HOLDER

064H177B	Holder H177B	(Chassis H147D) behind KBD
064H176	Holder H176	(Heat sink H33A)
064H092	Holder H92	(BENDER BOARD)
064H124	Holder H124	(BENDER BOARD)

COVER

065H135	Cover H135	(Top panel H142)
065H127B	Cover H127B	(Chassis H147D front)
065H126	Cover H126	(Slide Pot mask)
065H132	Cover H132	(BENDER BOARD slide Pot mask)
065H065	Cover H65	(Slide switch mask)

KNOB, BUTTON

016H098	Knob H98	(slider)
016H106	Knob H106	(rotary, BENDER BOARD)
016H102	Knob H102	(rotary, PANEL BOARD)
016H095	Button H95	(for SPQ009F)
016H085	Button H85	(White)
016H086	Button H86	(Purple)
016H087	Button H87	(Light blue)
016H088	Button H88	(Dark blue)
016H036	Button H36	(BENDER BOARD)

AC CORD SET

053H218	DC-320-J01	100V
053H219	UC-704-J01	117V 2P
053H220	EC-210-J06	220V 2P
053H221	EC-702-J05	240V 2P
053H222	SC-415-J06	240V 3P

SWITCH

13169503	ESE-3711	(VOLTAGE SELECTOR)
13149109	2wi XII	[POWER SWITCH (UL mark)]
13159322	HSW0372-01-520	(slide switch)
13129327	SPQ009F	(key switch)
13129717	KEH10003	(key switch, LFO-2)
13129531	SUT32A-1	(push switch, BEND)
13159138	SSS212B	(DIP)

JACK

13449125	HLJ0520-01-110	
13449126	HLJ0520-01-010	
13449226	HLJ4305-01-030	

SOCKET

13429615	TCS5350-01-1111	(DIN)
13429710	PA-126	(AC inlet 100V, 117V, 220V)
13429708	CM-3	(AC inlet 240V)
13439851	HA16R-3P	(XLR)
13429511	IC-49-2406 #2	(24P)

CONNECTOR

13439119	5045-03A
13439120	5045-04A
13439122	5045-06A
13439123	5045-07A
13438124	5045-08A
13439126	5045-10A
13439127	5045-11A
13439130	5046-03A
13439131	5046-04A
13439132	5046-05A

TRANSFORMER

022H056A	100V, 117V, 220V, 240V	(Power)
12449229	DP-101	(Matching)

FILTER

13529105	DSS310-55D223S	(Bypass capacitor)
12449229	FKOB-160MH15	(Coil)

DIODE

15019629	05Z6.2X	(zener)
15019617	05Z11X	(zener)
15019639	1SZ59	(zener)
15219403	5P05M(50V) or 5P4M(400V)	(SCR)
15019254	2B4B41	(bridge rectifier)
15019247	GP-30G	(Hi-Fi Special)
15019103	1S2473	
15029150	GL-9PR12	(LED, red, package white)
15029149	GL-9PG12	(LED, green, package white)
15029151	GL-9HY12	(LED, yellow, package white)
15029152	GL-9HD12	(LED, red, package white)
10529148	GL-9ND2	(LED, red/YG, package white)
15029147	GL-9HD2	(LED, red, high intensity package orange)
15029161	GL-9HD51A	
15029160	GL-9HD51 B or C	
15029162	BR5557K	(LED, red, high intensity package red)

all equivalent

ARRAY

15019116	DAP-601

FUSE

12559335	T-GGS1 (CSA)	1A	Prim. 100V, 117V
12559510	SEMKO T315mA		Prim. 220V, 240V
12559514	SEMKO T2A		sec. 220V, 240V
12559336	T-GGS2 (CSA)	2A	sec. 100V, 117V
12559337	T-GGS3 (CSA)	3A	sec. 100V, 117V
12559338	T-GGS3.15 (CSA)	3.15A	sec. 100V, 117V
12559516	SEMKO	T3.15A	sec. 220V, 240V

PCB

Order for PCB replacement will usually be filled with a newer one as long as they are compatible (if not, may be accompanied by adapting guide).

149H179C	CPU BOARD	(pcb 052H402C)
149H180B	MODULE BOARD (4-VOICE)	(pcb 052H403B)
149H181B	MODULE BOARD (2-VOICE)	(pcb 052H403B)
149H182A	BENDER BOARD	(pcb 052H404A)
149H183A	PANEL (L) BOARD	(pcb 052H405A)
149H184C	PANEL (R) BOARD	(pcb 052H406C)
149H186C	JACK BOARD	(pcb 052H408C)
162H061A	POWER SUPPLY BOARD (100V, 117V)	(pcb 052H409A)
162H062A	POWER SUPPLY BOARD (220V, 240V)	(pcb 052H409A)
149H191	FILTER BOARD (100V, 117V)	(pcb 052H416)
149H192	FILTER BOARD (220V, 240V)	(pcb 052H416)

POTENTIOMETER

	SLIDER	
13339420	S3018P405-B15	100KB
	ROTARY	
13219126	EVH-5XAP15-B15	100KB
13219125	EVH-5XAP15-B14	10KB
	TRIMMER	
13299563	RVG0707V101-10-103M	10K
13299564	RVG0707V101-10-104M	100K
13299562	RVG0707V101-10-503M	50K
13299525	3321P-1-502	5K

TRANSISTOR

15119108	2SA798-G
15119121	2SA937-Q or 2SA1115-E (15119129)
15119814	2SB1015-O
151291300G	2SC1583-G
15129119	2SC2021-Q or 2SC2603-E (15129140)
15129136	2SC2878-A
151291080A	2SC945 (NZ Selected)
15129827	2SD1406-O

CAPACITOR

13529103	DD111CH221J50J 220PF
13529102	DD600-257BC104Z12 0.1μF
13529104	DE7150F472MVA1 (Line bypass capacitor)

IC

15179318	P8051-318-0	CPU	CPU BOARD
15179319	P8051-319-0	CPU	MODULE BOARD
15179142	P8031 or P8051	CPU	

P8031 and P8051 without suffix number (-318 or -319)
Both have no internal program and need external PROM.
Common to CPU and MODULE BOARD.

P8051-318, P8051-319
Contains program to make external PROM unnecessary.
NOTE: Internal/External ROMs can be switched by EA terminal of CPU. See Circuit Diagram.

15159702	M54563P	8-Unit 500mA Source type darlinton transistor
15189136	M5218L	Dual low noise op amp
15199117	M5230L	Variable output voltage regulator
15159701	M54522P	8-Unit 400mA Darlington transistor array
15189155	M51201L	Voltage comparator
15169304	74LS04	Hex inverter
15169352	74LS40	Dual 4-input positive NAND buffer
15169353	74LS145	BCD-to-Decimal decoder/driver
15159503	TC40H000P	Quad 2-input NAND gate
15159504	TC40H002P	Quad 2-input NOR gate
15159506	TC40H138P	3-to-8-line decoder/demultiplexer
15159524	TC40H245P	Octal bus transceiver
15159507	TC40H273P	Octal D-type filp-flop
15159131	TC4053BP	Triple 2-channel multiplexer/demultiplexer
15159134	TC4028BP	BCD to decimal (binary to octal) decoder
15179317	TC5517APL or MB8416-25LP	RAM
15179316	TC5517AP or MB8416-25P	RAM

Use only "L" type for IC24 (CPU BOARD) for the longer battery life.

15189146	IR9022	Low power dual op amp
15229801	IR3109	VCF
15219130	ADC0803LCN	A/D Convertor
15179620	2732A-A	PROM A CPU BOARD

Unnecessary when CPU is P8051-318

15179621	2732A-B	PROM B MODULE BOARD
15159508	TC40H373P	Octal D-type latch (3-state output)

Unnecessary when CPU is P8051-319.

15189117	TL081C	OP AMP
15189118	TL082CP	OP AMP
15189154	TL064CP	Low power op amp
15159113	HD14051BP	8-Channel analog multiplexer/demultiplexer
15159313	MC14551B	Quad 2-input analogmultiplexer/demultiplexer
15159311	MC14504B	HEX level shifter
15219127	ITS80141	D/A Converter
15229810	CEM3340	VCO
15219129	CEM3360	VCA
15219124	μPC1252H2	VCA selected (white)
15199119	μPC3423C	Overvoltage protector
15219131	HA17903PS	Dual comparators
15229802	BA662-A	VCA
15229812	EHM-S226W83S	Hybrid amp
15159136	CD4067B	Single 16-Channel multiplexer/demultiplexer

PHOTO COUPLER

15229712	PC-900

RESISTOR

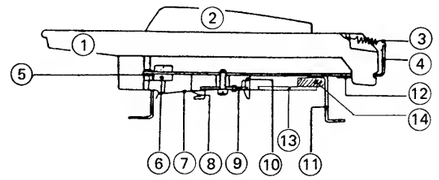
	CRB25FX (1%)		
13769162DO	3.6K		
13769263DO	4.99K		
13769173DO	10K		
13769177DO	15K		
13769178DO	16K		
13769180DO	20K		
13769181DO	22K		
13769185DO	33K		
13769188DO	43K		
13769191DO	56K		
13769197DO	100K		
13769200DO	130K		
13769264DO	140K		
13769201DO	150K		
13769203DO	180K		
13769205DO	220K		
13769213DO	470K		
13769221DO	1M		
	KNY2W		
13859106	(0.47Ω)		
13859107	(0.82Ω)		
	POSISTOR		
15229910	ERS-B33G122		
	ARRAY		
13919304	RM4-105J	1M	x 4
13910106	RM6-103K	10K	x 6
13919302	RM8-102J	1K	x 8
13919301	RM8-472J	4R7K	x 8
13829821	RM8-103K	10K	x 8
13919303	RM8-333J	33K	x 8
13919122	EXQ-D08E270J	27	x 8
13919317	EXQ-D08E680J	68	x 8
13919318	EXQ-D08E682J	6.8K	x 8
13919131	RM0889		
13919128	RM0688		
13919132	RM0891		
13919129	RM0689		
13919130	RM0690		

BENDER UNIT

2327571300	PB-6

KEYBOARD

004H008 SK-361C (61 keys)



KEYBOARD PARTS
SK-361C (004H008)

NO	PART NO	DESCRIPTION	
1	106H026	Natural key	C F
1	106H027	Natural key	D
1	106H028	Natural key	E B
1	106H029	Natural key	G
1	106H030	Natural key	A
1	106H031	Natural key	C' F'
2	106H032	Sharp key	black
3	070H029	Key spring	H29
4	061H086A	Chassis	H86A
5	068H004	Guide bushing	H4
6	101H141	Level felt	H141
7	071H044	Contact leaf	H44
8	071H051	Busbar 8P	H51
	071H054	Busbar 5P	H54
9	043H007	Switch unit 12P	H7
	043H008	Switch unit 13P	H8
10	104H029	Busbar holder	H29
11	062H024	Chassis bracket	H24
12	098H006	Key stopper	H6
13	052H283-5	Matrix board	H283-5
14	107H059	Cushion	H59

OTHERS

068H049	LED guide H49
073H027	LED spacer H27
048H033A	Heat sink H33A
125569111	CR 1/3N (Lithium battery)
12199519	TF-758 (Fuse holder)

THE MIDI

MIDI stands for Musical Instrument Digital Interface designed to enable interconnecting synthesizers, sequencers, rhythm machines, home computers, etc. Copies of publications concerning MIDI hardware and data format will be obtained from MIDI committee or through Roland distributers.
In the following listed are data formats and data handling capabilities of MIDI system of the JP-6 and other Roland models now on the market, for reference.

NOTE: Availability of MIDI effects at slave equipment depends on its MIDI operation scheme.

JP-6 MIDI INPLEMENTATION

TRANSMITTED DATA

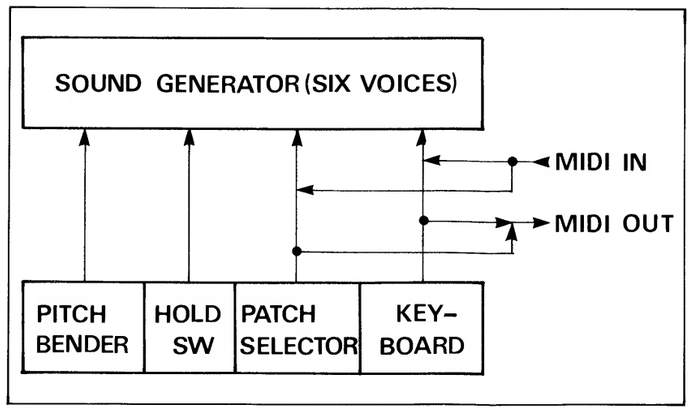
Status	Second	Third	Description
1001 000*	0kkk kkkk	0vvv vvvv	Note On (v=40H) / off (v=0)
1011 000*	127 (7FH)	0	POLY Mode Select (All notes off)
1100 0000	000p pppp		Program Change p=0 - 31 (1FH)
1111 0110			Tune

RECOGNIZED RECEIVE DATA

1001 000*	0kkk kkkk	0vvv vvvv	Note On (v > 0) / off (v=0) Velocity ignored
1000 000*	0kkk kkkk	0vvv vvvv	Note Off. Velocity ignored
1011 000*	125 - 127	0	Mode Select
1100 000*	000p pppp		Program Change
1111 110			Tune

Notes:

1. In WHOLE KEY mode, the JP-6 sends and receives on Channel 1 only. In SPLIT KEY mode, channels 1 and 2 are allocated to the upper half and the lower half of the keyboard respectively.
   In OMNI mode, any channel will be accepted.
2. The receiver accepts both OMNI and POLY Select.
   When MONO Select is received, the receiver switches to OMNI mode.
3. The key signal received from MIDI IN is mixed with self contained key signal.
4. The JP-6 accepts Program Changes not as the number of the tone program but as the number of a combination of Key Mode (WHOLE/SPLIT) and a tone Program Number.
   The receiver reads Program Changes when PATCH PRESET on the control panel is turned on.
5. The notes outside the JP-6 keyboard range will be shifted by octave(s) to fall within the range.



JP-6

JX-3P MIDI INPLEMENTATION

TRANSMITTED DATA

Status	Second	Third	Description
1001 0000	0kkk kkkk	0vvv vvvv	Note On (v=40H) / (v=0)
1011 0000	0100 0000	0	Hold Off from rear panel jack, if enabled.
1011 0000	0100 0000	7FH	Hold On from rear panel jack, if enabled.
1011 0000	0111 1111	0	POLY Mode Select (All notes off)
1100 0000	00pp pppp		Program Change from front panel, if enabled. Bank A-1 (0) → Bank D-16 (63)
1110 0000	0bb0 0000	0bbb bbbb	Pitch Bender if enabled.

	MSB	LSB
MAX (high)	127	96
CENTER	64	0
MIN (low)	0	0

Notes:

1. HOLD switch on the front panel does not send the signal to MIDI OUT.
2. Pitch Range (0kkk kkkk) is 36(C0) - 96(C5).
3. The transmitter sends All Notes Off (POLY Select) when all of the keys are released.

RECOGNIZED RECEIVE DATA

Status	Second	Third	Description
1001 0000	0kkk kkkk	0vvv vvvv	Note On (v > 0) / off (v=0) Velocity ignored.
1000 0000	0kkk kkkk	0vvv vvvv	Note Off. Velocity ignored.
1011 0000	0100 0000	0	Hold Off, if enabled.
1011 0000	0100 0000	7FH	Hold On, if enabled. v=1 - 126 ignored.
1011 0000	125 (7DH)	0	OMNI Select (All notes off).
1011 0000	127 (7FH)	0	POLY Select (All notes off).
1100 0000	00pp pppp		Program Change if enabled. p=0 - 63
1110 0000	0bb0 0000	0bbb bbbb	Pitch Bender if enabled.

	MSB	LSB
MAX	127	96
CENTER	64	0
MIN	0	0

LS 5 bits ignored.

Notes:

1. The JX-3P does not respond to MONO Mode Select.
2. Internal sequencer is not connected to MIDI out.
3. In OMNI mode, any channel will be accepted.
4. Sensitivity of the Pitch Bender is selected by the receiver.

	Wide	Middle	Narrow
MAX (MSB - 127 LSB - 96)	+7	+4	+2 semitone
MIN (MSB - 0 LSB - 0)	−7	−4	−2 semitone

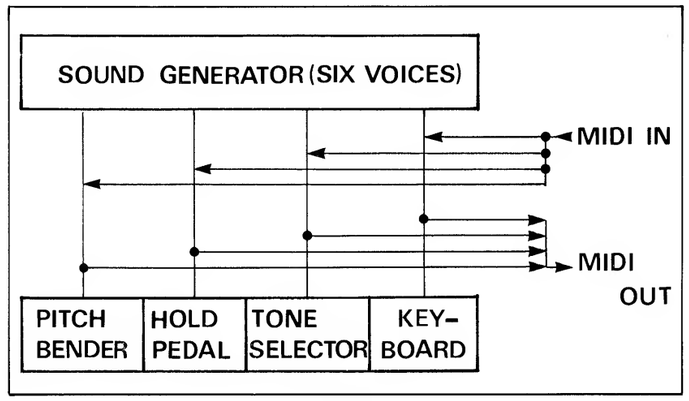
FRONT PANEL CODED FUNCTION

When power on, pressing a Program Select switch will disable the following functions.

Switch	Function
14	Hold On/Off, both transmit and receive.
15	Pitch Bender Change, both transmit and receive.
16	Program Change, both transmit and receive.

Note:

1. On power up, not pressing any switches, these MIDI functions are enabled.
2. The notes outside the JX-3P keyboard range will be shifted by octave(s) to fall within the range.



JX-3P

HP-300/400 MIDI INPLEMENTATION

TRANSMITTED DATA

Status	Second	Third	Description
1001 0000	0kkk kkkk	0vvv vvvv	Note On
		0000 0000	Note Off
			kkk kkkk = 29 - 103 (HP-300)
			21 - 108 (HP-400)
			vvv vvvv = 1 - 127
1011 0000	0100 0000	0111 1111	Damper On
		0000 0000	Damper Off
1011 0000	0100 0001	0111 1111	Soft On
		0000 0000	Soft Off
1011 0000	0111 1111	0000 0000	All Notes Off
			POLY Mode Select

RECOGNIZED RECEIVE DATA IN OMNI MODE

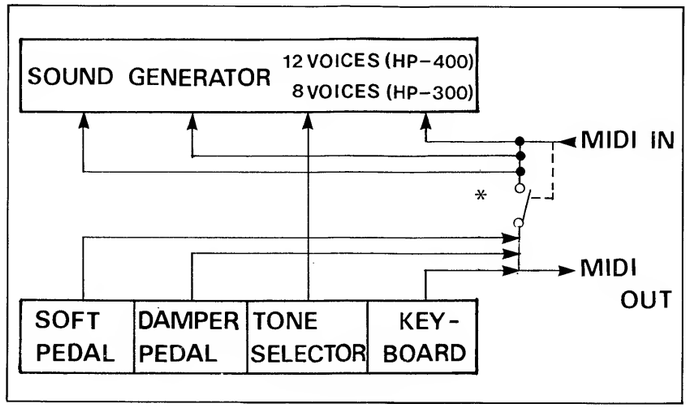
Status	Second	Third	Description
1000 xxxx	0kkk kkkk	0vvv vvvv	Note Off
			kkk kkkk = 0 - 127
			vvv vvvv = 0 - 127
			xxxx = 0 - 15
1001 xxxx	0kkk kkkk	0vvv vvvv	Note On
		0000 0000	Note Off
			kkk kkkk = 0 - 127
			vvv vvvv = 1 - 127
1011 xxxx	0100 0000	0111 1111	Damper On
		0000 0000	Damper Off
1011 xxxx	0100 0001	0111 1111	Soft On
		0000 0000	Soft Off
1011 0000	0111 1111	0xxx xxxx	All Notes Off
			POLY Mode Select
			xxx xxxx any value
	0111 1110	0xxx xxxx	All Notes Off
			MONO Mode Select (as OMNI)
	0111 1101	0xxx xxxx	All Notes Off
			OMNI Mode Select

RECOGNIZED RECEIVE DATA IN POLY MODE

Status	Second	Third	Descrption
1000 0000	0kkk kkkk	0vvv vvvv	Note Off
			kkk kkkk = 0 - 127
			vvv vvvv = 0 - 127
1001 0000	0kkk kkkk	0vvv vvvv	Note On
			Note Off
			kkk kkkk = 0 - 127
			vvv vvvv = 1 - 127
1011 0000	0100 0000	0111 1111	Damper On
		0000 0000	Damper Off
1011 0000	0100 0001	0111 1111	Soft On
		0000 0000	Soft Off
1011 0000	0111 1111	0xxx xxxx	All Notes Off
			POLY Mode Select
	0111 1110	0xxx xxxx	All Notes Off
			MONO Mode Select (as OMNI)
	0111 1101	0xxx xxxx	All Notes Off
			OMNI Mode Select

Notes:

1. The transmitter sends All Notes Off code when all the keys are released.
2. The received notes outside the HP-300 (400) keyboard range will be shifted by octave(s) to fall within the range.



HP-300, HP-400

* Engaging MIDI IN disconnects some of the intraconnections for optimum operation when linking sequencer.